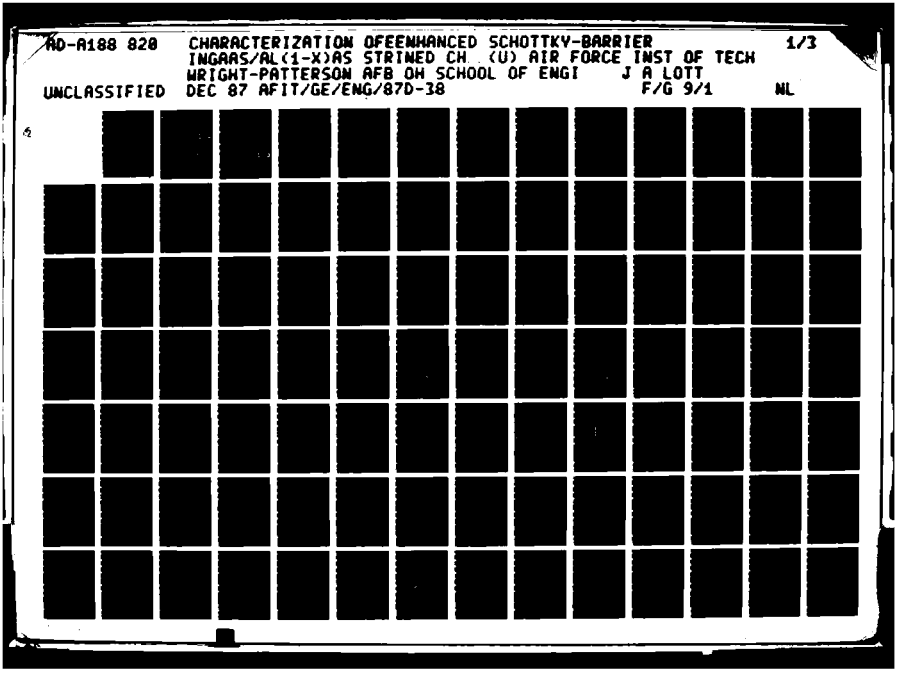
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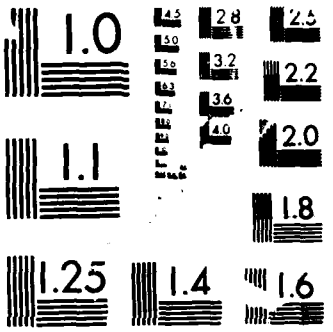

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CHARACTERIZATION OF ENHANCED SCHOTTKY-BARRIER InGaAs/$Al_xGa_{1-x}As$ STRAINED CHANNEL MODULATION-DOPED FIELD-EFFECT TRANSISTOR

THESIS

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Captain, USAF

AFIT/GE/ENG/87D-38

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THESIS

Presented to the Faculty of the School of Engineering

of the Air Force Institute of Technology

Air University

In Partial Fulfillment of the

Requirements for the Degree of

Master of Science in Electrical Engineering

James A. Lott, B.S.

Captain, USAF

December 1987

Preface

Enhanced Schottky-barrier $In_yGa_{1-y}As/Al_xGa_{1-x}As$ strained channel MODFETs were fabricated with and without graded n-$Al_xGa_{1-x}As$ barrier layers. A classical-statistics, charge-control model was formulated to design the MBE-grown substrates, upon which the MODFETs were fabricated. The classical model was compared to an exact quantum mechanical model developed at The University of Michigan. Both the models and DC measurements confirmed an increase in the effective Schottky-barrier height of the devices. The enhanced Schottky-barrier MODFETs exhibited extremely high transconductances and microwave performance.

I am deeply indebted to Professor Hadis Morkoç and his students and post-doctorates at the Coordinated Sciences Laboratory, University of Illinois at Urbana-Champaign. Specifically, I would like to acknowledge and express my sincerest appreciation to Tim Henderson for the MBE-growth of the substrates; Jim Chen for assisting in the device fabrication; and Dr. Hilmi Unlu for many useful discussions.

Next, I would like to acknowledge the assistance of Professor Jasprit Singh and Mark D. Jaffe of The Center for High Frequency Microelectronics, The University of Michigan at Ann Arbor. I am extremely grateful to them for their enlightening discussions on the theoretical aspects of strained channel MODFETs, and for modifying their quantum model in order to simulate my devices.

Sincere thanks also go to Dr. Timothy J. Drummond of Sandia National Laboratories, Albuquerque, NM for his expert advise and assistance in understanding MODFET device structures.

I would like to acknowledge and thank several individuals from the Air Force Avionics Laboratory, Microwave Device Group, for their assistance in performing the microwave

measurements and in using the microwave circuit modelling software. My thanks goes to Chris Bozada, Jim Gillespie, Tom Jenkins, Stu Labovitz, Mike Paulus, and Rick Worley.

I was fortunate to have a thesis committee with broad, distinguished backgrounds. Specifically I'd like to respectively acknowledge Major (Professor) Donald R. Kitchen, my thesis chairman, for his ceaseless guidance and encouragement, discussions on semiconductor materials and microwave devices, and his critical review of the manuscript. Also, I'm extremely grateful to Dr. Cole W. Litton, my sponsor from the Air Force Avionics Laboratory, for his innumerable discussions, daily encouragement, and coordination of my laboratory work. Dr. Litton's insights and expertise were without parallel. I would also like to express my thanks to Major (Professor) Edward S. Kolesar for the many challenges and knowledge he's given me, both in this thesis and in his classroom. Also, sincere appreciation goes to Captain (Professor) Randy J. Jost for his critical review of the manuscript and assistance with the microwave measurements.

Finally, I wish to thank my parents and family for their support from California. And most importantly, I'd like to thank my friends Marcie, Renee, and Amity, to whom this thesis is dedicated.

James A. Lott

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List of Symbols

Symbol	Description	Unit
a	Constant	volt-cm^2
a	Equilibrium lattice constant	Å
a	Hydrostatic deformation potential	eV
b	Shear deformation potential	eV
$\mathbf{b}_I$	Burger's vector	Å
C_{dg}	Parasitic drain-to-gate capacitance	fF
C_{ds}	Parasitic drain-to-source capacitance	fF
C_{gs}	Parasitic gate-to-source capacitance	pF
C_{ij}	Elastic stiffness coefficients	dyn/cm^2
$\partial E_o/\partial P$	Hydrostatic pressure coefficient	eV/dyn cm^{-2}
$\Delta a_\perp$	Lattice constant mismatch perpendicular to an interface	Å
$\blacktriangle E_c$	Conduction band discontinuity	eV
ΔE_c	Conduction band discontinuity	Volts
ΔE_{F0}	Constant (equals zero at 300 °K)	Volts
ΔE_{F1}	Energy difference between E_F and the bottom of the quantum well at the hetero-interface	Volts
ΔE_{F2}	Equilibrium Fermi level in AlGaAs	Volts
ΔE_{hh}	Change in bandgap due to tensile strain	eV
ΔE_{lh}	Change in bandgap due to compressive strain	eV
ΔE_v	Valence band discontinuity	eV
d_g	Thickness of the graded n-AlGaAs epitaxial barrier layer	Å
d_p	Thickness of the p^+-GaAs epitaxial layer	Å
D_i	Two-dimensional density of states of the i^{th} sub-band	states/unit area

Symbol	Description	Unit
ε	Permittivity	F/cm
ε_o	Permittivity of vacuum	F/cm
ϵ	Misfit strain	unitless
E	Electric field	Volts/cm
E_c	Conduction band energy level	eV
E_v	Valence band energy level	eV
E_F	Fermi energy level	eV
E_g	Energy bandgap	eV
Φ	Work function	Volts
ϕ_B	Schottky-barrier height	Volts
ϕ_B*	Effective Schottky-barrier height	Volts
ϕ_i	Built-in voltage	Volts
f(E)	Fermi-Dirac distribution function	unitless
f_{max}	Maximum frequency of oscillation	GHz
f_T	Unity forward current gain frequency	GHz
g_m (or GM)	Extrinsic transconductance	mS
g_{mo}	Intrinsic transconductance	mS
G_{max}	Maximum available power gain	dB
GMAX	Maximum available power gain	dB
G_d	Parasitic drain conductance	mS
h	Planck's constant	J-s
h_{21} (or H21)	Forward current gain	unitless
$\hbar$	Reduced Planck's constant ($h/2\pi$)	J-s
I_D (or ID)	Drain current	mA
I_G (or IG)	Gate current	mA

Symbol	Description	Unit
κ	Constant or fitting factor	unitless
k	Boltzmann's constant	J/°K
K	Stability factor	unitless
L_d	Parasitic drain inductance	pH
L_g	Parasitic gate inductance	pH
L_s	Parasitic source inductance	pH
L_G	Gate length	μm
μ_n	Electron mobility	$cm^2/V\text{-}s$
m*	Effective mass	kg
N_c	Effective density of states in the conduction band	cm^{-3}
N_v	Effective density of states in the valence band	cm^{-3}
N_A	Acceptor impurity density	cm^{-3}
N_D	Donor impurity density	cm^{-3}
NF	Noise figure	dB
n (or n_{free})	Free electron density	cm^{-3}
n_i	Electron density in the i^{th} sub-band	cm^{-3}
n_s	2DEG density	cm^{-2}
n_{so}	2DEG equilibrium density	cm^{-2}
ρ	Charge density	cm^{-3}
ρ	Linear density of misfit dislocations	cm^{-1}
p (or p_{free})	Free hole density	cm^{-3}
q	Fundamental unit of charge	Coul
qV	Electrostatic potential (in energy units)	eV
R	Radius of curvature	m
R_d	Parasitic drain resistance	Ω

Symbol	Description	Unit
R_g	Parasitic gate resistance	Ω
R_i	Parasitic intrinsic resistance	Ω
R_s	Parasitic source resistance	Ω
R_C	Contact resistance	Ω
R_S	Large-signal source resistance	Ω
S_{ij}	S-parameter	unitless
τ	Electron transit time from drain to source	psec
t	Thickness	cm
υ	Poisson ratio	unitless
υ_s	Saturation velocity	cm/s
V	Electrostatic potential	Volts
V_D (or VD)	Applied drain voltage	Volts
V_{DS} (or VDS)	Applied drain-to-source voltage	Volts
V_G (or VG)	Applied gate voltage	Volts
V_{OFF}	Threshold voltage	Volts
x	AlAs mole fraction	unitless
ψ	Wavefunction	unitless
y	InAs mole fraction	unitless
Ω	Ohm	Ω
W	Depletion region width	μm
χ	Electron affinity	Volts
Z	Gate width	μm

Abstract

Enhanced Schottky-barrier $In_{0.15}Ga_{0.85}As/Al_xGa_{1-x}As$ pseudomorphic modulation-doped field-effect transistors (MODFETs) were fabricated with 1.2 μm gate-lengths on MBE-grown substrates. The effective gate Schottky-barrier height was enhanced by adding a thin p^+-GaAs layer beneath the gate. A portion of the n-$Al_{0.15}Ga_{0.85}As$ barrier layer beneath the p^+-GaAs surface layer was linearly graded from a mole fraction of 0.15 to 0.30 to further increase the effective Schottky-barrier height. MODFETs of identical dimension and doping density were fabricated without the p^+-GaAs and/or graded n-$Al_xGa_{1-x}As$ layers for comparison. The goal was to improve the MODFET's high-frequency performance by reducing the gate leakage current. The effective Schottky-barrier height was shown to increase from 0.9 to 1.6 volts for the p^+-graded samples. The extrinsic transconductance was as high as 190 mS/mm for the p^+-graded samples and 311 mS/mm for the graded control samples. The p^+-graded samples exhibited an f_T and f_{max} of 26 and 54 GHz, respectively, compared to 19 and 28 GHz, respectively, for the graded control samples. The noise figure for the p^+-graded samples was 1.7 dB at 12 GHz, compared to 1.9 dB for the graded control samples. Overall, the MODFETs with enhanced Schottky-barriers significantly outperformed control devices with unenhanced barriers. Also, this is the first time that enhanced Schottky-barriers have been successfully reported for pseudomorphic MODFETs. A first-order charge-control model was derived to design the MODFET structures by solving the Poisson equation with appropriate boundary conditions. This model is compared to the classical charge-control model based on a numerical solution of Poisson's equation and the Maxwell-Boltzmann approximation to the Fermi-Dirac distribution function. This model produces energy band and charge distribution diagrams for a given MODFET structure. The models are shown to have excellent quantitative agreement with the measured results.

CHARACTERIZATION OF ENHANCED SCHOTTKY-BARRIER $InGaAs/Al_xGa_{1-x}As$ STRAINED CHANNEL MODULATION-DOPED FIELD-EFFECT TRANSISTORS

I. Introduction

Background

The study of modulation-doped semiconductor heterostructures is now one of the most interesting and active fields in semiconductor device physics. The pioneering work of Esaki and Tsu in 1969 [30] and Dingle et al. in 1978 [22] concerning superlattice heterostructures has led to the rapid development of several new opto-electronic and microwave semiconductor devices. A promising and widely studied new microwave device is the modulation-doped field-effect transistor (MODFET). A MODFET was recently shown to operate at 230 GHz, the highest ever reported for a three-terminal transistor [88]. The MODFET, also called a high electron mobility transistor (HEMT), a two-dimensional electron gas field-effect transistor (TEGFET), and a selectively-doped heterojunction transistor (SDHT), was first reported in the open literature in 1980 by Fujistsu Ltd. [61]. Like metal-semiconductor field-effect transistors (MESFETs), the MODFET consists of two ohmic contacts (source and drain) and a Schottky-barrier gate (Fig. 1.1). The gate controls the flow of current between the source and drain contacts.

The difference between MODFETs and MESFETs, and the key to the MODFETs improved performance, resides in the underlying semiconductor material. MODFETs are fabricated on an $Al_xGa_{1-x}As/GaAs$ heterostructure that is grown by either molecular-beam epitaxy (MBE) or metalorganic chemical-vapor deposition (MOCVD) [25]. The motion of

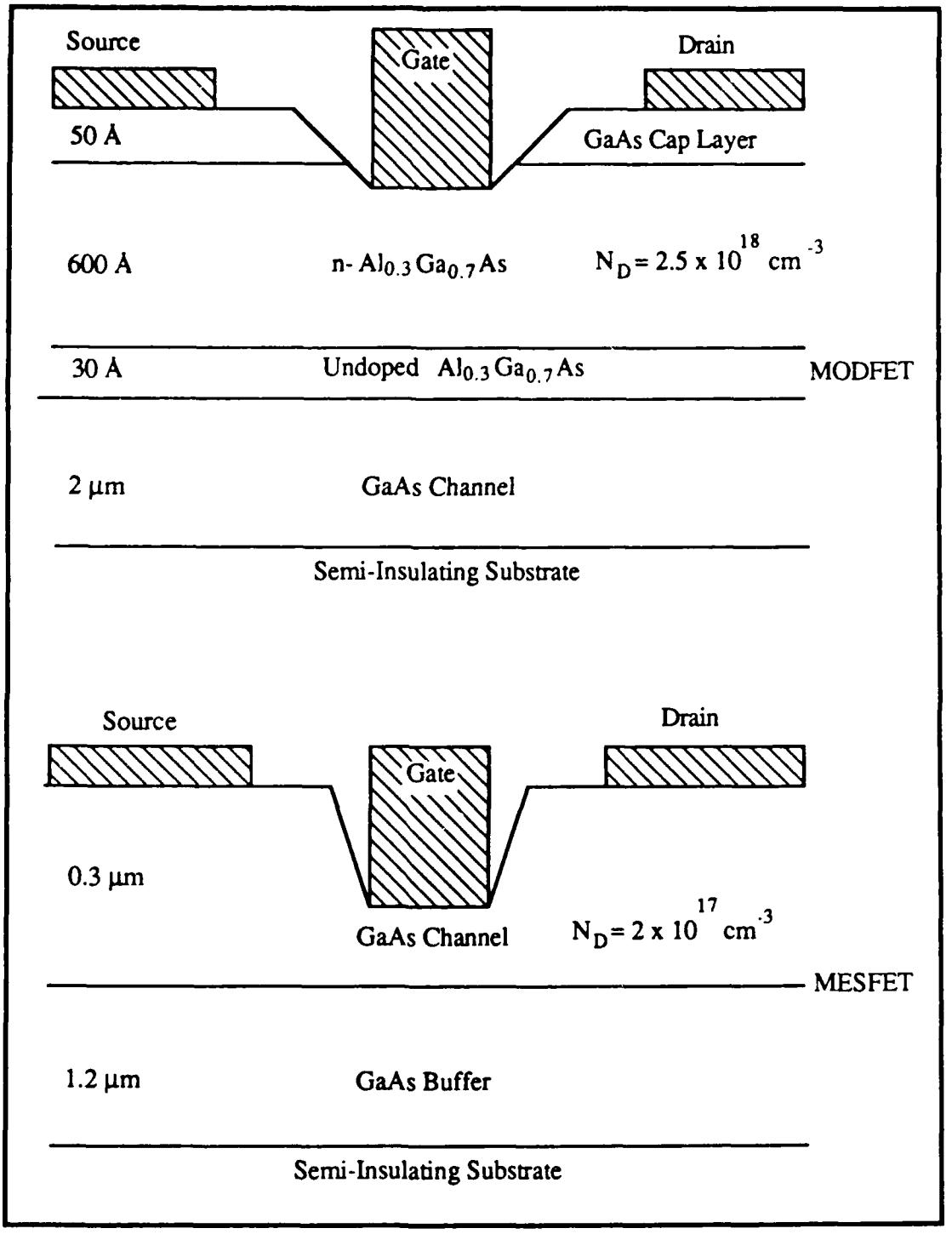

Fig. 1.1 The Structure of a MODFET and a MESFET used for Research [4:1399]

charge-carriers is confined to a thin sheet (called a two-dimensional electron gas or 2DEG) within the GaAs epitaxial layer which is similar to the inversion layer formed at the SiO_2/Si interface of a metal-oxide-semiconductor field-effect transistor (MOSFET). The 2DEG is contained in a quantum-potential well at the $Al_xGa_{1-x}As$/GaAs heterojunction. The quantum-potential well is a result of the conduction band discontinuity (e.g. energy barrier) at the heterojunction. Electrons from donors in the higher bandgap $Al_xGa_{1-x}As$ material diffuse into the quantum-potential well in the narrow bandgap GaAs material forming the 2DEG. The 2DEG is about 100 Å or less thick and forms the carrier channel that links the MODFET's source and drain. The separation of these electrons from the ionized donors greatly reduces impurity scattering resulting in a high electron mobility and saturation velocity. Compared to GaAs MESFETs with similar or even smaller gate lengths, the MODFET exhibits higher: electron mobility, sheet carrier concentration, electron saturation velocity, transconductance, cut-off frequency [87:107], and noise figure [88:140].

Motivation

One critical problem with the MODFET is its inability to support gate voltages larger than the Schottky-barrier gate height without incurring significant amounts of leakage current. The maximum allowable gate voltages for these devices is limited to approximately 0.8 - 1.0 volts due primarily to: tunneling mechanisms at the heterojunction, thermionic leakage current at the Schottky-barrier gate, and parasitic conduction in the n-AlGaAs layer [53]. The relatively low breakdown voltage of the gate Schottky-barrier limits MODFET power handling capabilities [81:1023]. A thin p^+ beryllium-doped GaAs layer has been added between the n-$Al_xGa_{1-x}As$ layer and the metal gate. This modified device was called an enhanced Schottky-barrier (ES)MODFET. The p^+-GaAs layer increased the forward-biased gate turn-on voltage from 0.8 volts in the normal MODFET to as high as 1.6 volts in the (ES)MODFET [70:175]. A similar MODFET with a graded bandgap $Al_xGa_{1-x}As$ layer

and p^+-GaAs surface layer was fabricated by Ohata et al. [67]. The device was shown to have improved high frequency noise performance over normal MODFETs.

The term "normal MODFET" refers to the model $Al_xGa_{1-x}As$ (n-doped)/ GaAs (intrinsic) system, which has been by far the most widely studied [25:780]. Other systems in which the modulation doping concept has been demonstrated include: InP/ $Ga_{0.47}In_{0.53}As$, $Al_{0.48}In_{0.52}As/Ga_{0.47}In_{0.53}As$ [25:776; 76], $In_{0.15}Ga_{0.85}As/GaAs$ [73], $In_yGa_{1-y}As/Al_xGa_{1-x}As$ [35; 36; 46; 47; 73; 76], $Si_{1-x}Ge_xSi$ [18], and others. The primary motivation for using the $Al_xGa_{1-x}As/GaAs$ system is that the $Al_xGa_{1-x}As$ lattice is matched to the GaAs lattice over the entire compositional range. This feature permits the formation of high quality heterojunctions which are not dominated by misfit dislocations.

Recently significant attention has been given to the $In_yGa_{1-y}As/Al_xGa_{1-x}As$ pseudomorphic or strained-quantum well MODFET (Fig. 1.2). The use of the $In_yGa_{1-y}As/Al_xGa_{1-x}As$ heterojunction system over the $Al_xGa_{1-x}As/GaAs$ system has two main advantages. First, since InGaAs has a lower bandgap than GaAs, a lower AlAs mole fraction (x = 0.15 with InGaAs; x = 0.30 with GaAs) can be used in the $Al_xGa_{1-x}As$ while still maintaining the necessary conduction band discontinuity (approximately 0.3 volts) for a high 2DEG sheet carrier density (approximately 10^{12} cm^{-2}) [46: 564]. This means that persistent photoconductivity (PPC) effects and uncontrollable threshold voltage shifts associated with high mole fraction ($x \geq 0.2$) $Al_xGa_{1-x}As$ below 77 °K can be eliminated or reduced. The PPC effects lead to "collapse" of drain current-voltage (I-V) characteristics and are believed to be caused by deep level electron traps (D-X centers) in the silicon-doped $Al_xGa_{1-x}As$ [46:564]. The $In_yGa_{1-y}As/Al_xGa_{1-x}As$ avoids these problems by using a low AlAs mole fraction ($x \leq 0.2$) where the D-X occupation probability is significantly reduced. Also, the low AlAs mole fraction $Al_xGa_{1-x}As$ can be doped to higher densities due to reduced donor compensation and exhibits a larger Schottky-barrier height as compared to a normal MODFET [46]. Second, the $In_yGa_{1-y}As$ system has higher saturation velocities and

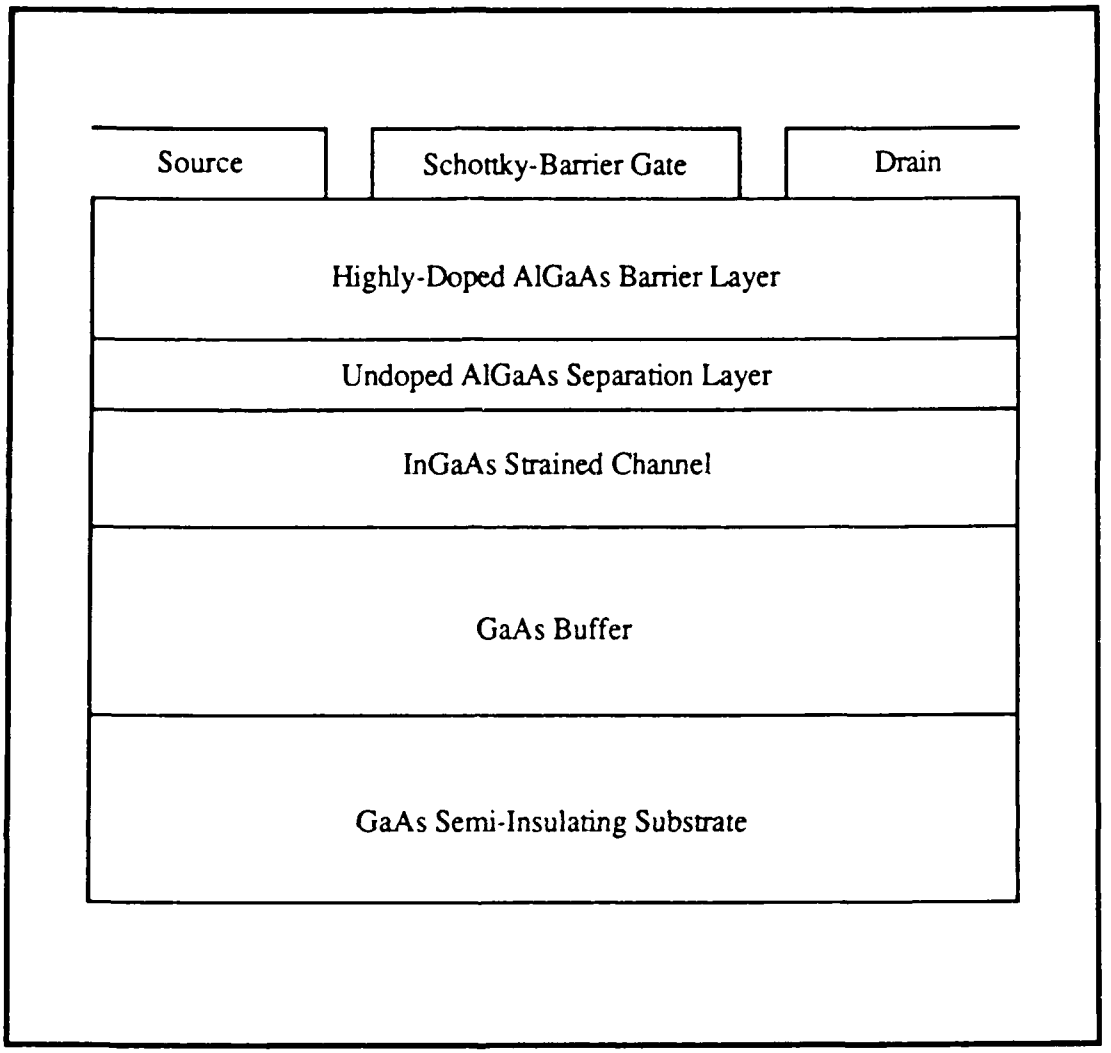

Fig. 1.2 The General Structure of an InGaAs Pseudomorphic MODFET

improved carrier confinement in the quantum-potential well. However, there is a lattice mismatch of approximately 1 percent between a GaAs buffer layer and an $In_{0.15}Ga_{0.85}As$ quantum-well layer (Fig. 1.2). The $In_{0.15}Ga_{0.85}As$ is grown thin enough (approximately 200 Å) so that the lattice strain is taken up coherently (accommodated as elastic strain) by the quantum-well layer resulting in a dislocation-free "pseudomorphic" material. Device

performance rivaling the best reported $Al_xGa_{1-x}As$/GaAs MODFETs has been demonstrated with the pseudomorphic MODFET [47]. The placement of a highly doped p^+-GaAs layer on the pseudomorphic MODFET to enhance the Schottky-barrier gate height and improve microwave performance was recently accomplished [60]. The result was unexpectingly a reduced Schottky-barrier gate turn-on voltage and was attributed to strain induced by the pseudomorphic quantum-potential well layer [60:6-2]. Also, diffusion of Be dopant atoms during device fabrication was thought to have lowered the gate's barrier height.

According to Morkoç [64], the pseudomorphic MODFET will have a major impact on supercomputers, telecommunications, and space exploration. High-speed, low-noise amplifiers are needed for very low-level radio signal reception [55]. The low-noise performance means that the device can detect weak signals from spacecraft and satellites. It also makes it possible to transmit military communications at levels that are difficult for others to intercept. The following study was directed at refining the pseudomorphic MODFET.

Problem Statement

The purpose of this thesis was to characterize the DC and microwave performance of enhanced Schottky-barrier InGaAs/$Al_xGa_{1-x}As$ strained channel MODFETs. The goal was to increase the effective Schottky-barrier height of the devices and observe the resulting effect on device performance. An increase in the MODFET's effective Schottky-barrier height was expected to reduce leakage current at the gate for a given applied gate voltage. This would improve the microwave power capabilities of the MODFET and permit higher gate voltage swings in MODFET logic circuits.

Approach

The first approach was to add a p^+-GaAs surface layer to the pseudomorphic MODFET to raise the Schottky-barrier height at the gate. The second approach was to linearly grade the bandgap of a portion of the n-$Al_xGa_{1-x}As$ barrier layer. Increasing the n-$Al_xGa_{1-x}As$ bandgap should have theoretically raised the Schottky-barrier gate height (along with the p^+-GaAs layer). The linear grading of the n-$Al_xGa_{1-x}As$ layer was also an attempt to relieve the lattice-strain caused by the mismatched morphology of the $In_yGa_{1-y}As$/ $Al_xGa_{1-x}As$ and $In_yGa_{1-y}As$/ GaAs heterointerfaces. The modified MODFET device was designed to first-order by deriving and applying one-dimensional charge-control equations. Next, the MODFET was fabricated using established lithography, etching, and metallization techniques, and then characterized by experimental DC and microwave measurements. The graded-bandgap devices with p^+-GaAs surface layers were compared to graded bandgap control samples grown on the same substrate with the p^+-GaAs surface layers etched away. Also for comparison, graded-bandgap samples were grown without p^+-GaAs surface layers. Finally, ungraded bandgap samples were grown to the same dimensions and doping densities as their graded bandgap counterparts. The device performance was measured and compared to existing MODFETs.

Scope

Pseudomorphic $In_yGa_{1-y}As/Al_xGa_{1-x}As$ MODFETs with gate lenghts of 1.2 μm were fabricated at the University of Illinois (UI) Coordinated Sciences Laboratory. Substrate epitaxial layers were grown by molecular-beam epitaxy (MBE). MODFETs were then fabricated on the prepared substrates using established photolithography, etching, and metallization processes. A p^+-GaAs surface layer was added beneath the pseudomorphic MODFET gate during MBE-growth. In concert with recommendations from previous MODFET research [53], the bandgap of the $Al_xGa_{1-x}As$ layer was graded. The effect on

MODFET performance of a linear grading distribution scheme and p^+-GaAs surface layer was predicted by a derived, first-order (one-dimensional) charge-control model. The model was used to design MODFET layer thicknesses and doping levels. The model was also compared to a quantum mechanical model recently developed at The University of Michigan. Predicted results from each of the models were compared to the measured MODFET DC and microwave performance via several figures of merit. The figures of merit included the following: source resistance (R_S), contact resistance (R_C), transconductance (g_m), unity current gain frequency (f_T), maximum frequency of oscillation (f_{max}), and noise figure (NF).

Assumptions

Several assumptions were used in this study to derive first-order (one-dimensional) charge-control models for the proposed MODFET structures. These assumptions are listed in Appendices A and B. The assumptions used to derive a revised classical charge-control model are listed in Appendix F. Additionally, the following general assumptions were made:

1) The MBE-grown substrates prepared by personnel at the University of Illinois were of high crystalline quality and grown exactly to the specifications listed in Table 3.3;

2) The pseudomorphic approximation is valid for the MODFETs fabricated in this work so that strain is limited to the InGaAs channel epitaxial layer.

Results

Enhanced Schottky-barrier pseudomorphic MODFETs with gate lengths of 1.2 μm were successfully fabricated. The devices with graded n-$Al_xGa_{1-x}As$ barrier and p^+-GaAs (enhanced) surface layers exhibited extrinsic transconductances (g_m's) as high as 190 mS/mm. The graded-unenhanced samples had g_m's as high as 311 mS/mm. The

effective Schottky-barrier height increased from 0.8 to 1.5 eV and from 0.9 to 1.6 eV by the addition of a 100 Å p^+-GaAs surface layer on the ungraded and graded samples, respectively. The graded-enhanced samples exhibited an f_T and f_{max} of 26 and 54 GHz, respectively, compared to 19 and 28 GHz, respectively, for the graded-unenhanced control samples. The noise figure (NF) performance of the enhanced Schottky-barrier samples was superior to the NF performance of the unenhanced samples, both in the graded and ungraded case. A NF of 1.7 dB at 12 GHz was measured for a graded-enhanced sample, compared to an NF of 1.9 dB at 12 GHz for the corresponding graded-unenhanced sample.

Sequence of Presentation

This thesis is divided into six chapters and six supporting appendices. Chapter I introduces the pseudomorphic MODFET, states a research objective, and provides a plan of attack. Chapter II describes the background information on MODFET structures, operating principles, and characteristics. It is intended to provide the reader with a knowledge base and perspective on the thesis research. In Chapter III, material parameters of strained channel MODFETs are presented. Also, design principles of pseudomorphic MODFETs are discussed, and the results of a derived (first-order) charge-control model are presented. The model was used to design the MBE-grown substrate material used in this work. Next, Chapter IV describes the experimental procedures used to fabricate and characterize the enhanced Schottky-barrier pseudomorphic (ESP)MODFETs. The measured results presented in Chapter IV are then analyzed in Chapter V. Also, a revised classical charge-control model is presented and compared to an exact quantum mechanical charge-control model developed at The University of Michigan. Finally, conclusions and recommendations for further study are presented in Chapter VI.

II. Modulation-Doped Field-Effect Transistors

This chapter serves both as a review of the literature and as an introduction to the basic principles of the modulation-doped field-effect transistor (MODFET). It is intended to give the reader the background required to understand and appreciate the results of this study. In this chapter, the structure and fabrication of the normal MODFET is first introduced. The principles of MODFET operation are then presented by describing: modulation-doped heterojunctions, quantum potential-wells, charge transport via a two-dimensional electron gas (2DEG), and the enhanced mobility of superlattice structures. Next, first-order charge-control equations that model MODFET charge-transport and device operation are reviewed. The current-voltage (I-V) and microwave characteristics of MODFETs are then discussed. Next, the structure and fabrication of enhanced Schottky-barrier (ES) MODFETs is introduced by first presenting the rationale for device modification, and then the results of previous efforts. Finally, the structure and fabrication, and measured characteristics of the InGaAs/$Al_xGa_{1-x}As$ pseudomorphic MODFET are reviewed. A summary comparing experimental and commercially available MODFETs concludes the chapter.

MODFET Structure and Fabrication

The MODFET is a device which requires abrupt heterojunction and doping profiles. MODFET fabrication involves two distinct processing sequences. First, a thin film growth technique such as molecular-beam epitaxy (MBE), is used to grow epitaxial layers of varying binary and ternary compositions and dopant distributions. MBE is an ultrahigh vacuum (10^{-10} Torr) semiconductor deposition technique with control on the atomic scale of both the dopants and constituents forming the semiconductor epitaxial layers [90:333]. The epitaxial layers are grown on chromium-doped, semi-insulating (S.I.) GaAs substrates that are about 30 mils thick [25:792]. Second, individual MODFETs are defined on the

grown epitaxial layers by using lithography, etching, and metallization techniques similar to those used for MBE-grown metal-semiconductor field-effect transistors (MESFETs). The details of substrate preparation and growth [27] and device isolation and fabrication [25; 60] are available in the literature.

A MODFET structure was shown in Fig. 1.1. The structure and dimensions of a commercially available MODFET (Gould's MPD-H503) is shown in Fig. 2.1 for comparison. The two structures will serve as examples for MODFET device fabrication. The modulation-doped $Al_xGa_{1-x}As/GaAs$ heterostructural layers are grown on 2 inch, S.I., (100) GaAs liquid-encapsulated crystal (LEC) substrates [87:107]. Epitaxial layer deposition is performed by MBE at about 630 °C, one wafer at a time. Typical epitaxial layer growth rates are 1 μm/hr [87:109]. First, a 0.6 - 3.0 μm thick (typically 1 μm) unintentionally doped GaAs buffer layer is grown. This provides a high quality, defect-free interface on which the next layers of material are grown [69:16]. The background ionized acceptor concentration of the GaAs buffer layer is about 10^{14} cm^{-3} [25:777], which is negligible compared to the electron concentration in the 2DEG (about 10^{18} cm^{-3}). An undoped $Al_xGa_{1-x}As$ separation layer 0 - 90 Å is next, followed by an n-type $Al_xGa_{1-x}As$ barrier layer 300 - 600 Å thick. This $n\text{-}Al_xGa_{1-x}As$ layer is nominally silicon-doped to 2×10^{18} cm^{-3}. Finally, an n^+-type GaAs cap layer, 0 - 500 Å thick, is grown on the $Al_xGa_{1-x}As$. The GaAs cap layer is nominally silicon-doped to 3×10^{18} cm^{-3} and helps form ohmic contacts to the MODFET's source and drain [88:140]. Alternately, the $n\text{-}Al_xGa_{1-x}As$ may be graded down to GaAs near the surface [81:1018].

The second MODFET processing sequence is the fabrication of individual field-effect transistors (FETs) on the MBE-grown epitaxial layers. The FET fabrication process is illustrated in Fig. 2.2. The steps used to fabricate individual devices includes: lapping, mesa etching, source and drain contact metallization and alloying, gate recessing, gate metallization, and overlay metal evaporation.

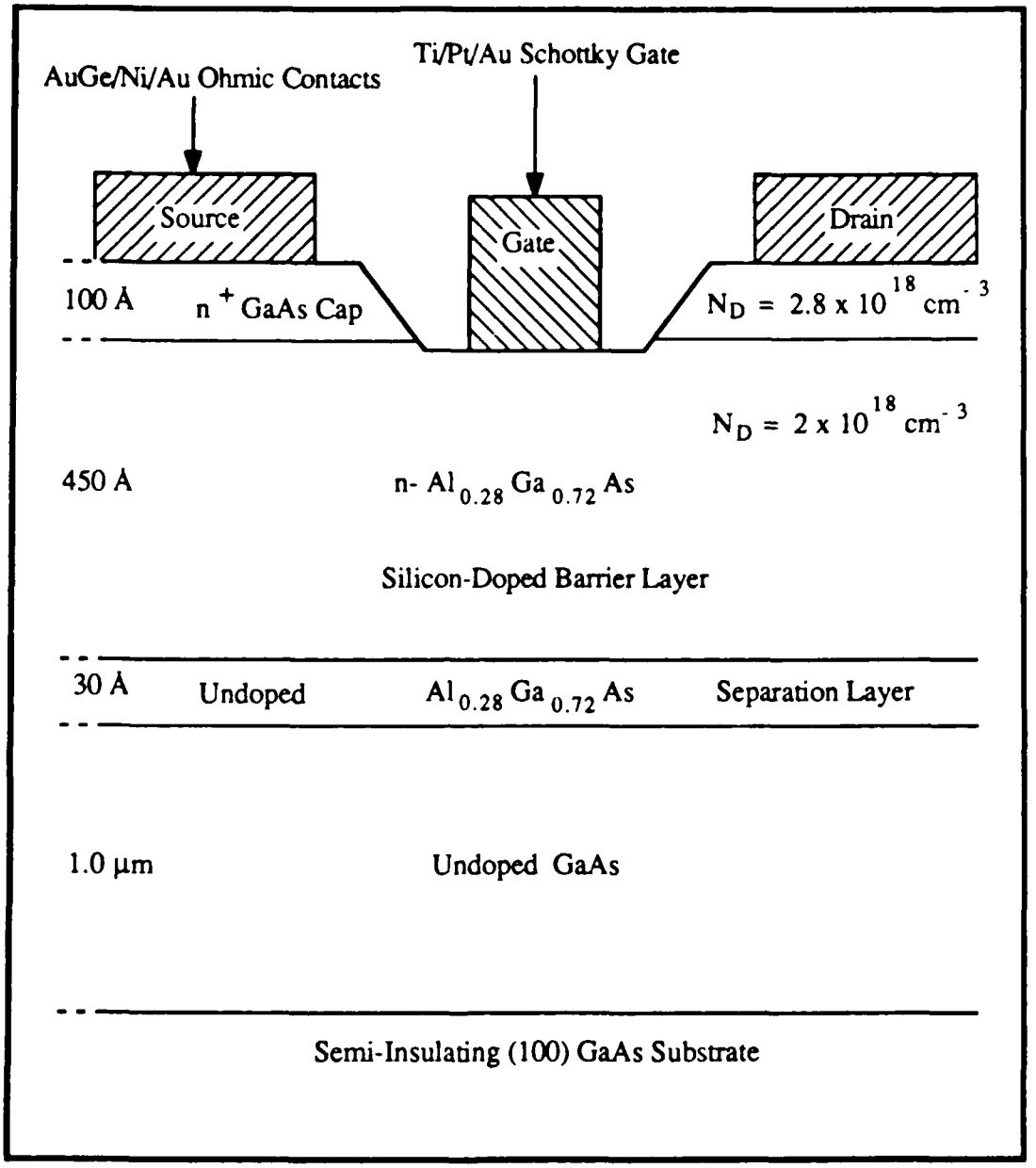

Fig. 2.1 Structure and Dimensions of Gould's MPD-H503 MODFET [87:109]

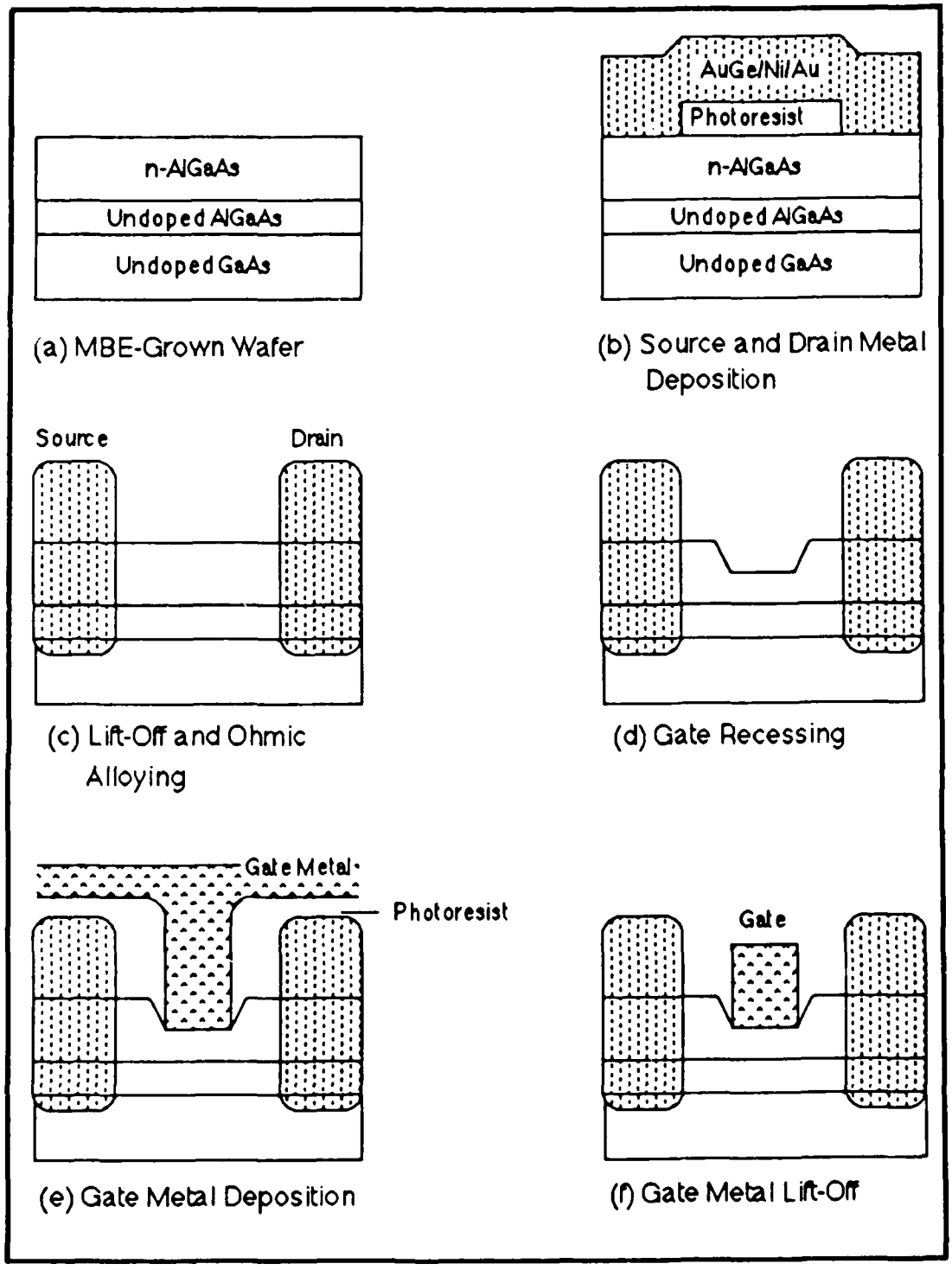

Fig. 2.2 MODFET Fabrication Process [60:2-5]

After MBE-growth, the individual wafers are lapped (thinned) to 350 - 400 μm [60:B-3]. The commercially available MODFET does not require lapping [87:109]. Mesa isolation patterns are defined lithographically and etched with a 3:1:1 DI H_2O:H_2O_2:HF solution [4:1399]. This leaves mesas of active material separated by non-conducting regions. Source and drain regions are then defined in positive resist and AuGe/Ni/Au contacts are evaporated. The metal is patterned and alloyed at 400 - 500 °C for 30 - 60 seconds in hydrogen atmosphere. The alloying allows Ge atoms to diffuse isotropically into the active epitaxial layers, past the $Al_xGa_{1-x}As$/GaAs heterojunction, and into the GaAs buffer layer. The result is a highly ohmic contact connecting the source and drain metallizations to the 2DEG charge-carrying channel. Nominal 1 μm gate channels are defined using chlorobenzene-treated photoresist (AZ4110) [46:565; 60:B-8]. Next, a wet chemical etch is used to recess the gate region below the GaAs cap layer. Alternately, reactive ion etching or ion milling may be used for gate recessing [65:34]. This step is immediately followed by evaporation of about 3000 Å of aluminum. The extent of the recess is dependent upon whether depletion or enhancement mode devices are desired. Finally, a thick Ti/Au overlay metallization [46:565] is deposited forming bonding pads. The Schottky-barrier gate metal may also be Ti/Pt/Au [87:109]. Gate geometries are typically 0.25 - 2.0 μm gate-length and 50 - 290 μm gate-width. The metallization pattern for the MPD-H503 MODFET is shown in Fig. 2.3. Submicron gate-length geometries require electron-beam lithography for the definition of all levels. A tri-layer resist technique has been used for electron-beam lithography of 0.25 μm x 50 μm MODFETs [88:142] and is detailed in [12].

Principles of MODFET Operation

The MODFET is similar to the (MESFET) (see Fig. 1.1). However, due to different physical mechanisms of carrier transport, the MODFET is markedly different from the

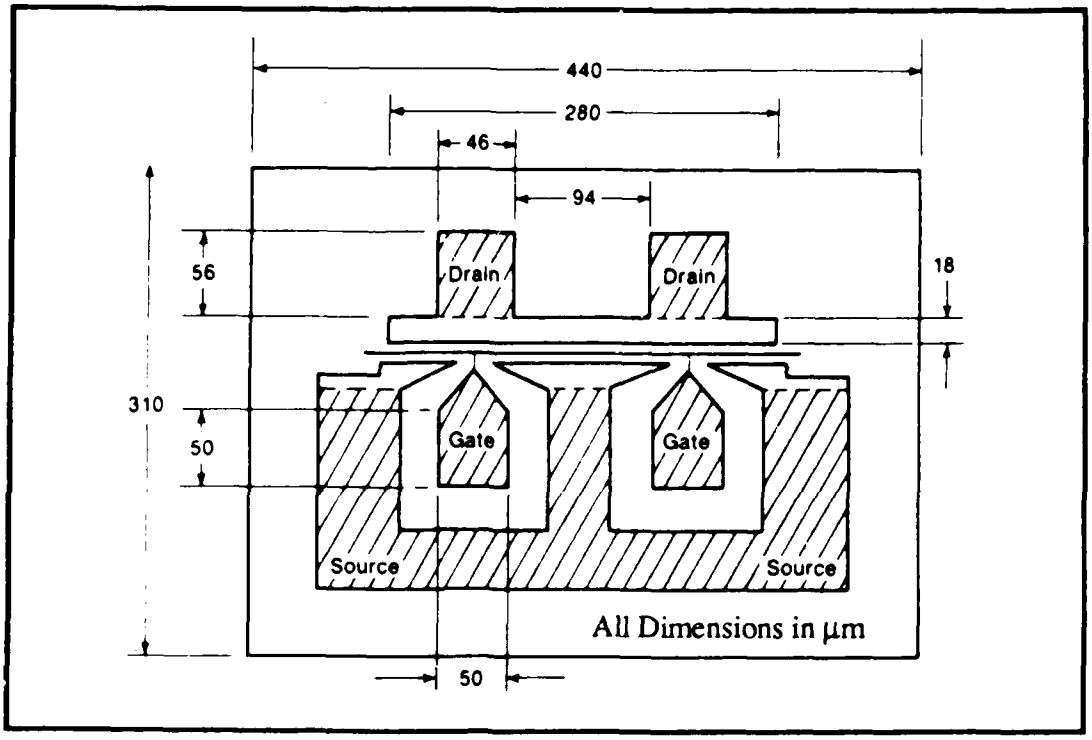

Fig. 2.3 Metallization Pattern for Gould's MPD-H503 MODFET [87:109]

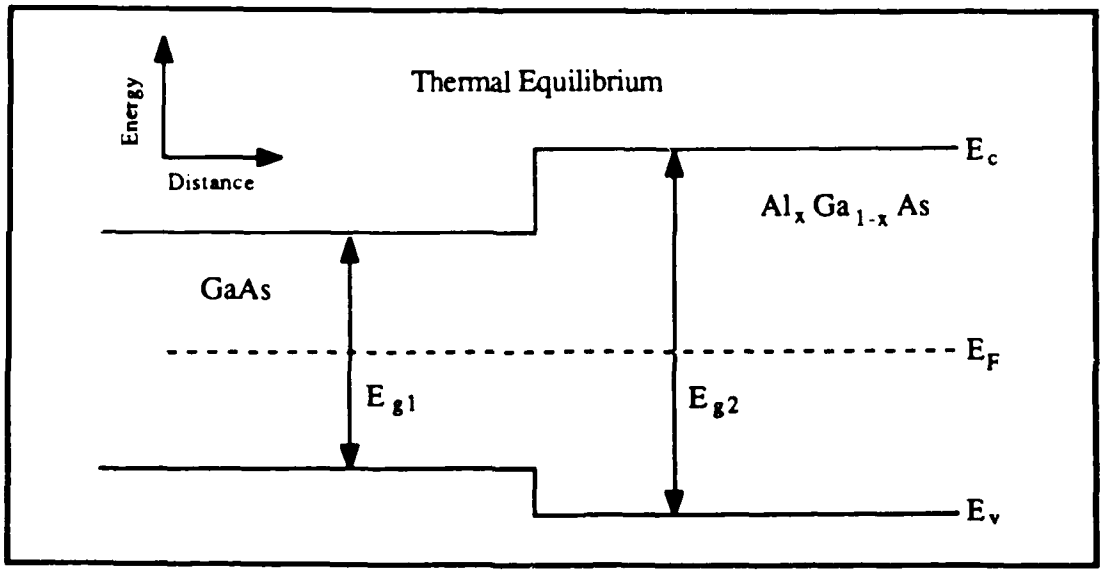

Fig. 2.4 Ideal Energy Band Diagram of an Undoped $Al_xGa_{1-x}As/GaAs$ Heterojunction

MESFET in its principle of operation. In a MESFET, the channel layer is a uniformly doped layer of a bulk semiconductor. Electrons and donors share the same space and interact via their Coulomb potentials. The effect of the Coulombic interaction on transport is known as ionized impurity scattering [89:27-30]. To maintain high channel current levels while decreasing device dimensions, the channel layer must be highly doped. This leads to increased impurity scattering and increased device noise [25:776]. In a MODFET, a heterojunction composed of Si-doped AlGaAs and undoped GaAs is used. Because of the conduction band discontinuity between the high bandgap AlGaAs and lower bandgap GaAs (e.g. energy barrier), electrons donated to the AlGaAs layer diffuse to the GaAs layer. A localized sheet of charge becomes trapped in a quantum potential well on the GaAs side of the heterointerface and forms a thin (less than 100 Å) quasi-two-dimensional electron gas (2DEG) layer [88:139]. Since there are no donor atoms intentionally present in the undoped GaAs layer, the electrons in the 2DEG layer do not undergo impurity scattering. The result is a device with a channel mobility approaching that of undoped bulk GaAs. The phonon scattering limited mobility in undoped GaAs is 8500 - 9000 cm^2/volts-s [81:1017] at 300 °K. Mobilities in excess of 10^6 cm^2/volts-s at 4 °K have been reported by several laboratories [25:774].

Unlike the MESFET, the MODFET functions more like a metal-oxide-semiconductor field-effect transistor (MOSFET). The Schottky-barrier gate controls the number of electrons in the 2DEG by raising and lowering the interface barrier. In a MESFET, bias applied to the gate modulates the channel's resistance and thereby the number of electrons passing through it. With a MODFET, the channel thickness remains constant; it is the number of carriers that is modulated.

Modulation-Doped Heterojunctions. A heterojunction is a junction formed between two dissimilar semiconductors [89:122]. The ideal energy band diagram of an undoped $Al_xGa_{1-x}As$/GaAs heterojunction in thermal equilibrium is shown in Fig. 2.4. The bandgap

energy (E_{g1}) of GaAs at 300 °K is 1.42 (eV) [89:849]. The bandgap energy of $Al_xGa_{1-x}As$ (E_{g2}) varies with the AlAs mole fraction x, and at 300 °K is given by [77:R9]

$$E_{g2}(x) = 1.424 + 1.247x \ \text{(eV)} \qquad (0 \le x \le 0.45)$$
$$= 1.424 + 1.247x + 1.147(x - 0.45)^2 \qquad (0.45 \le x \le 1) \tag{2.1}$$

The expressions in (2.1) are power series approximations to the $Al_xGa_{1-x}As$ bandgap. The Fermi level (E_F) lies near the middle of the bandgap for the undoped structure of Fig. 2.4. A modulation-doped heterojunction consists of an abrupt junction between two semiconductors which have different electron affinities, and in which the semiconductor with the smaller affinity is doped n-type [25:776]. The energy band diagram of an anisotype abrupt heterojunction ($Al_xGa_{1-x}As$ (*n*-doped)/GaAs (undoped)) is shown in Fig. 2.5. Discussions on similar heterojunctions, based on Anderson's energy band model for Ge/GaAs, have been published [15; 80:136; 74:283; 89:123-126]. Each semiconductor is characterized by its electron affinity χ, energy band gap E_g, and work function Φ. When the two semiconductors are brought into contact under thermal equilibrium, the Fermi level must coincide on both sides and the vacuum level is everywhere parallel to the band edges and is continuous (except at the heterointerface). The conduction band (E_c) has a discontinuity at the heterointerface where $\Delta E_c = q\chi_1 - q\chi_2$ [25:776]. The total built-in voltage (ϕ_i), which is set-up by the charge in the depletion region, is equal to the difference in work functions. As the composition x increases in $Al_xGa_{1-x}As$, its bandgap increases rapidly for $x \le 0.45$. For $x \le 0.45$, the conduction band discontinuity ΔE_c is given by the difference between the bandgaps of GaAs and $Al_xGa_{1-x}As$ (ΔE_g) multiplied by approximately 65 percent (and ΔE_v is approximately $0.35\Delta E_g$) [11:1064; 41:925]. Excitation and absorption spectroscopy have been used to determine the conduction band

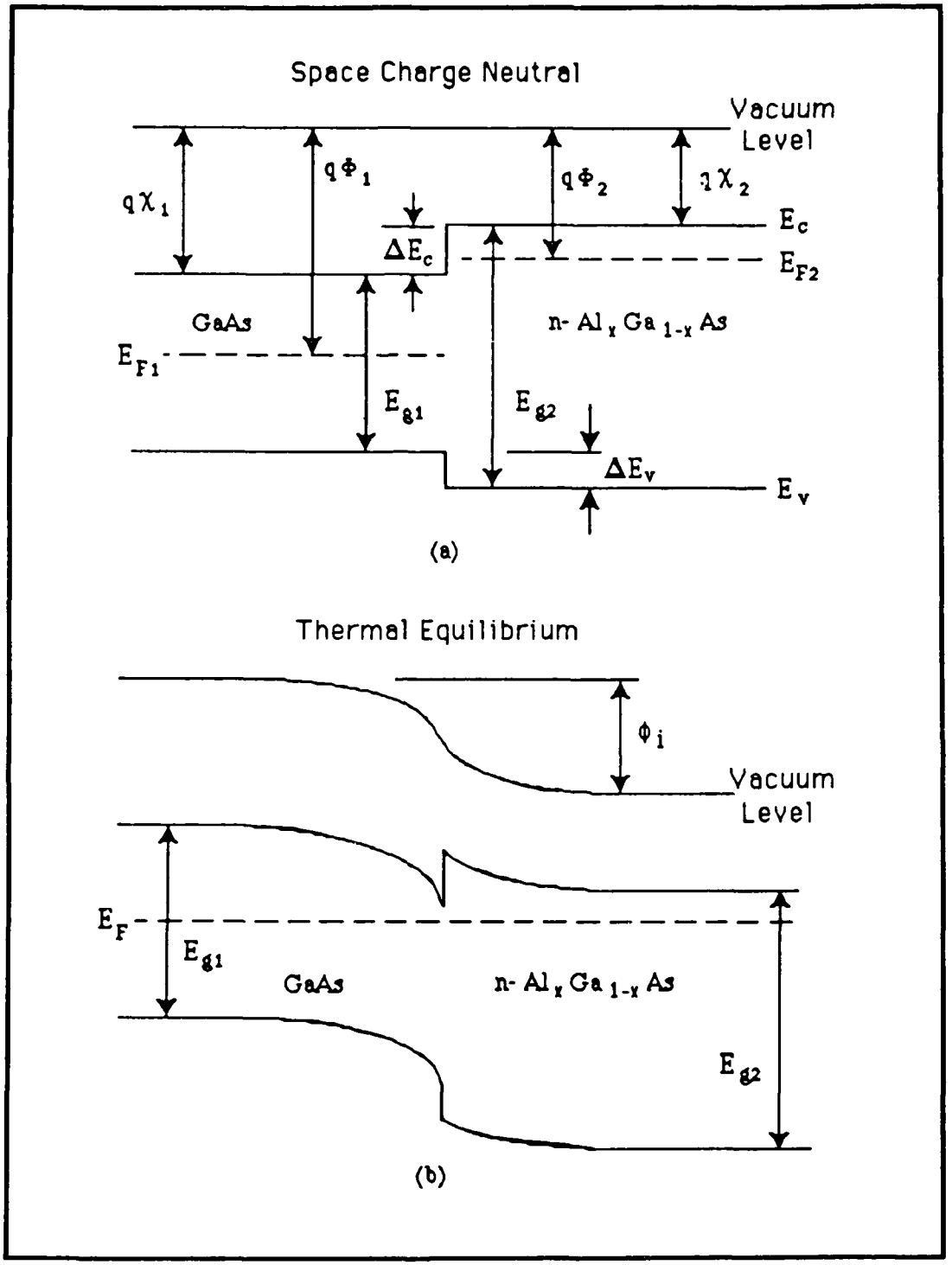

Fig. 2.5 Energy Band Diagram of an Anisotype n-$Al_xGa_{1-x}As$/GaAs (undoped) Abrupt Heterojunction [15:263]

offsets [3:64]. Optical absorption research and related theories have shown that $\blacktriangle E_c = 0.85\Delta E_g$ [3:64; 56:162; 98:155]. Recent modelling [93:618] of single quantum-well structures and excitation spectroscopy experiments on parabolic and square multi-period quantum-wells [3:64] have given $\blacktriangle E_c \approx 0.6\Delta E_g$ (where ΔE_g is the direct energy bandgap difference). For $x \geq 0.45$, $\blacktriangle E_c$ decreases so that the highest barrier to real space electron transfer possible at an $Al_xGa_{1-x}As/GaAs$ heterointerface occurs when $x = 0.45$ [41:925]. Alternately, $\blacktriangle E_c$ may be decreased or entirely eliminated by compositionally grading the $Al_xGa_{1-x}As$ (e.g. x goes to 0) near the heterointerface [11; 15]. The conduction band-edge may move below the Fermi level at the heterointerface if the $Al_xGa_{1-x}As$ is heavily doped n-type (e.g. 10^{18} cm^{-3}), and $\blacktriangle E_c$ is large. The GaAs becomes degenerate at the heterointerface if $E_F > E_c$.

The conduction band diagram of a single interface $Al_xGa_{1-x}As/GaAs$ modulation-doped heterojunction at thermal equilibrium is shown in Fig. 2.6. The permittivities of GaAs and $Al_xGa_{1-x}As$ are given as ε_1 and ε_2, respectively. The thickness of the $Al_xGa_{1-x}As$ separation layer is given as d_1, the Fermi energy level (E_F) is taken as a reference, and E_0 and E_1 represent the lower two allowed sub-band energies of the 2DEG. As previously noted, electrons originally introduced into the $Al_xGa_{1-x}As$ layer diffuse to the lower energy GaAs layer where they are confined due to the energy barrier at the interface. Ideally, charge transfer only requires that a discontinuity of greater than $\approx$ 2kT appears in the conduction band, and not a difference in bandgaps [25:776]. The region of the $Al_xGa_{1-x}As$ that is depleted of electrons forms a positive space charge region which is balanced by the sheet of electrons (2DEG) confined at the heterointerface. The resulting electric field perpendicular to the interface reaches values over 10^5 V/cm [81:1016] and causes severe band bending. The electron energies of the 2DEG are increased by their quantum-mechanical confinement, and discrete quantum sub-bands are formed. Each sub-band corresponds to a discrete state of the electron's perpendicular momentum (e.g. to a discrete

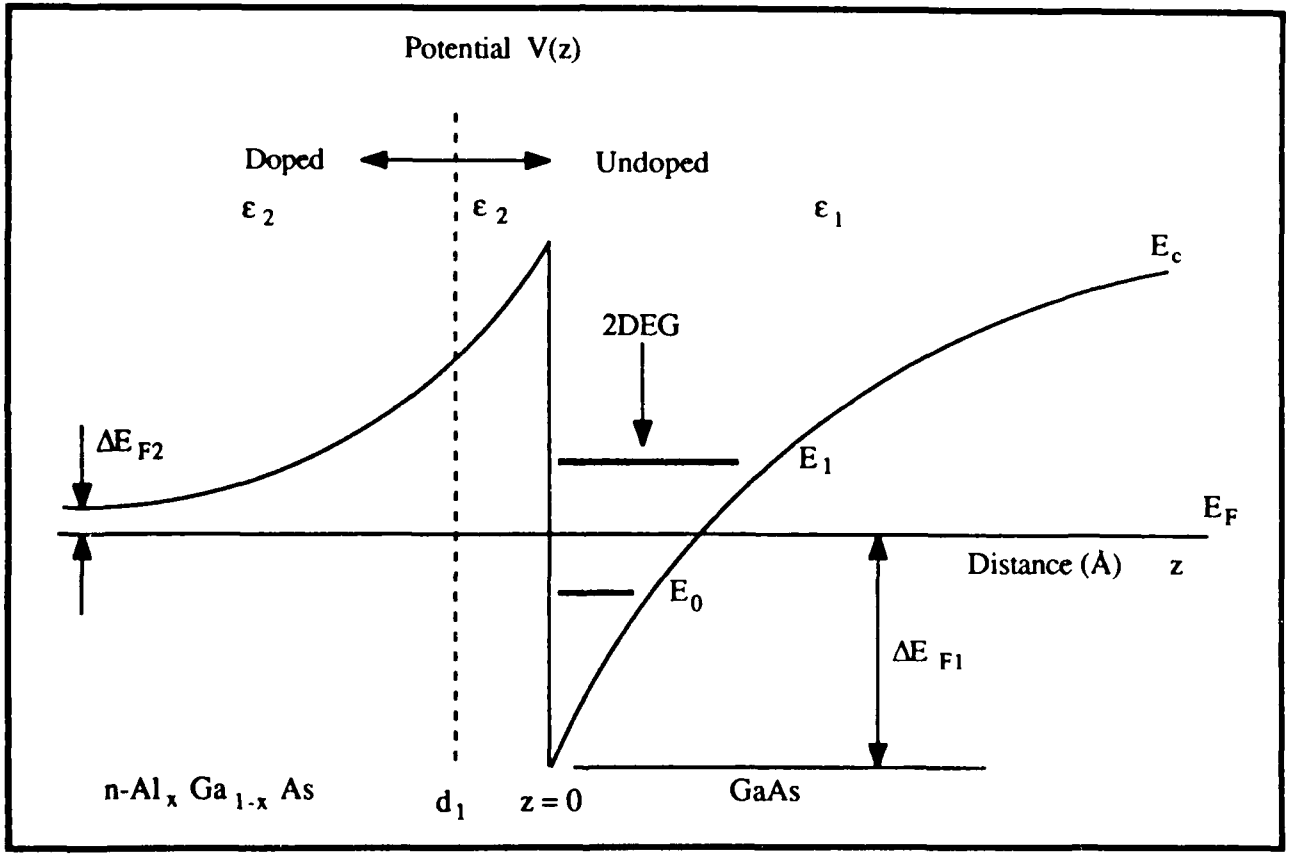

Fig. 2.6 Conduction Band Diagram of an $Al_xGa_{1-x}As$ /GaAs Heterostructure at Thermal Equilibrium (Energy Reference is the Fermi Level E_F) [25:776]

number of standing waves in the electron wave function [25:776]). Usually, only the two lowest sub-bands are appreciably populated [25:776]. (The next sub-section takes a closer look at the quantization of the 2DEG.)

The electrons and their donors are spatially separated but their close proximity allows an electrostatic interaction called Coulomb scattering. An undoped separation layer is added to further separate donors from the heterointerface. The thicker the separation layer d_1, the lower the Coulombic scattering and the higher the 2DEG mobility in the GaAs buffer layer. However, as d_1 increases, the density of the 2DEG decreases due to reduced electron transfer. The amount of electron transfer is determined by the donor density in the $Al_xGa_{1-x}As$, the $Al_xGa_{1-x}As/GaAs$ conduction band discontinuity, and the thickness of the separation layer. The conduction band discontinuity (ΔE_c), as previously stated, is a function of the AlAs mole fraction x in the $Al_xGa_{1-x}As$ layers. The quantization, density, and mobility of the 2DEG in modulation-doped layers has been investigated and is expanded upon in the following three sub-sections.

One-Dimensional Quantum-Wells. The spatial electronic distribution of a movable electron gas is described in general by the Schrödinger (wavefunction) and Poisson (charge density) equations [6:2]. When electrons in semiconductors are confined to move within a region surrounded by potential barriers, their energies undergo additional quantization [74:169]. According to L. Esaki [45:1]:

> In general, if characteristic dimensions such as superlattice periods and widths of potential wells in semiconductor nanostructures are reduced to less than the electron mean free path, the entire electron system will enter a quantum regime of reduced dimensionality with the presence of nearly-ideal heterointerfaces.

An example is shown in Fig. 2.7, where two quantum-potential-wells of different depths (one for electrons and the other for holes) are formed within an $Al_xGa_{1-x}As/GaAs/Al_xGa_{1-x}As$ heterostructure. The potential barriers to the electrons in the rectangular

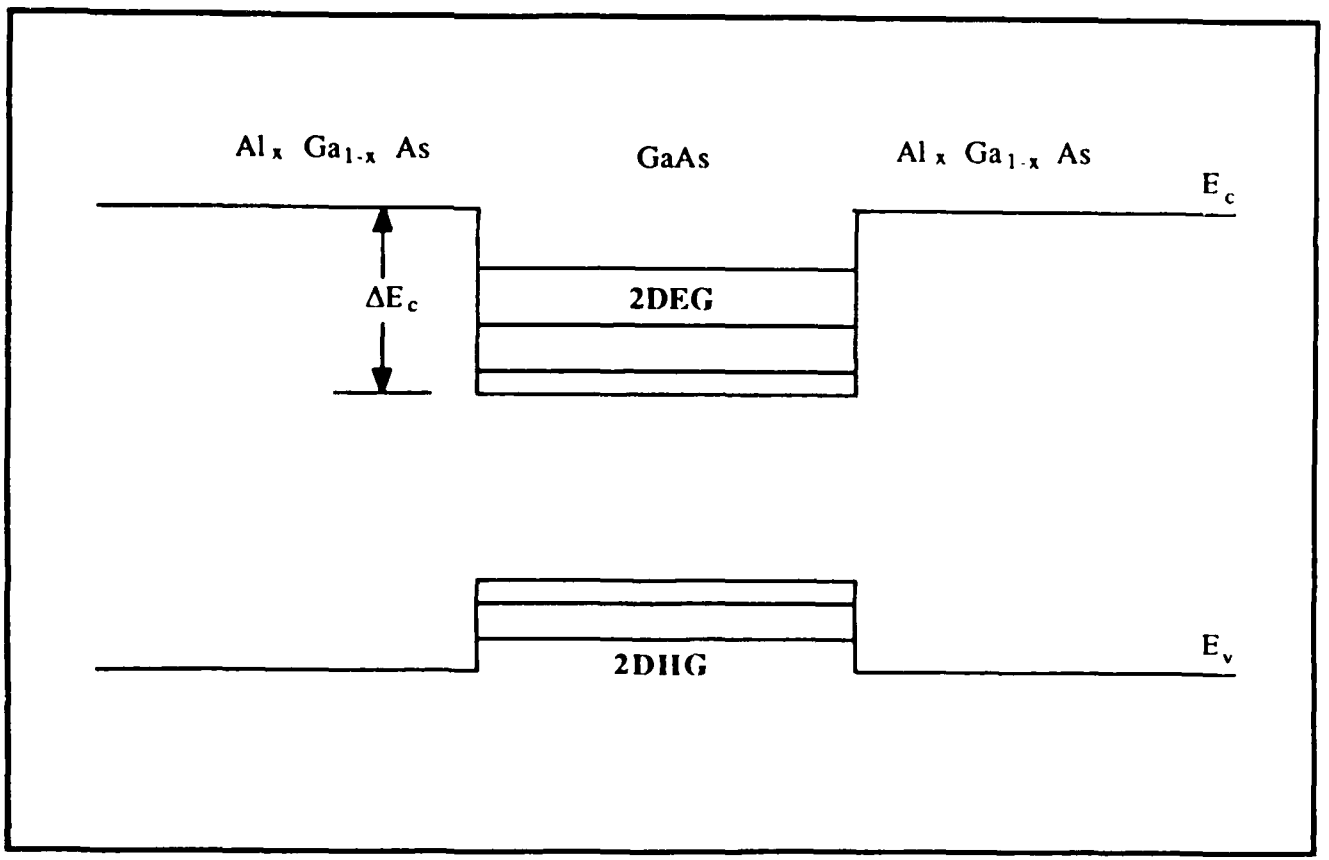

Fig. 2.7 An $Al_xGa_{1-x}As/GaAs$ Quantum-Well Heterostructure [74:171]

quantum-well are equal to the conduction band discontinuity (ΔE_c) between $Al_xGa_{1-x}As$ and GaAs. If one assumes the potential barrier is infinitely high (and assumes tunneling does not occur), the one-dimensional Schrödinger equation can be readily solved to obtain the eigenenergies (or allowed energy levels or states) within the quantum-well [6:137]. If the two rectangular barriers are a distance L apart (z-direction), the particles are free to move along the xy-plane while their z-direction energies (E_n) are quantized [74:169] and are given by [7:179]

$$E_n = \frac{(n+1)^2\pi^2\hbar^2}{2m^*L^2} \quad , \quad n = 0, 1, 2, \ldots$$

where m* is the effective mass. Thus the energies of the electrons and holes depend on the geometrical factor L. Equations for the allowed energy levels in parabolic, asymmetric triangular, and symmetric triangular quantum-wells may be found in [6:2-4].

The allowed energy levels of the 2DEG in a normal MODFET is often modelled as an infinite potential-barrier (asymmetric) triangular-well. This leads to the Airy equation with solution (for the quantized energies parallel to the heterointerface) [6:4; 21:956; 72:678]

$$E_n = \left(\frac{\hbar^2}{2m^*}\right)^{1/3}\left[\frac{3\pi qE_z}{2}\left(n+\frac{3}{4}\right)\right]^{2/3} \quad , \quad n = 0, 1, 2, \ldots$$

where E_z is the electric-field perpendicular to the heterointerface, and m* is the effective electron mass. The electron and hole (heavy and light) effective mass depends on the direction of travel (important when making assumptions in order to derive a charge-control model for the MODFET) [42]. Similarly, it is known that the strong electric-field at the SiO_2/Si interface of a MOSFET (quasi-triangular quantum-well) confines the charge carriers to a thin layer (100 Å or less) and consequently boundary quantization arises

[6:41]. Motion parallel to the interface is hardly affected and quasi-two-dimensional behavior results.

A MODFET that has a V-shaped quantum-well is described in [75]. It will be shown, via a conduction band diagram, that the pseudomorphic MODFET consists of a quasi-rectangular quantum-well, and thus is able to confine the 2DEG more effectively than the quasi-triangular-well of the normal MODFET.

Two-Dimensional Electron Gas (2DEG). Electrons in an n-channel MODFET are confined at the heterojunction in a quasi-triangular potential well (refer to Fig. 2.6). The energy reference in the quantum well is the bottom of the well at the heterointerface. The width of the well at the Fermi level (E_F) is about 100 Å [25:276]. The confined electrons form a quasi-2DEG. The 2DEG travels in a direction that is parallel to the heterojunction interface under the influence of an electric field between MODFET source and drain. For a typical gate length-to-width geometry of 1-to-280 μm, respectively, the thickness of the 2DEG is negligible. Thus the 2DEG density, n_s, is given in areal units of cm^{-2}.

A fundamental problem in analyzing the MODFET is the accurate estimation of the 2DEG density at the modulation-doped $Al_xGa_{1-x}As/GaAs$ heterojunction [98:154]. The most accurate approach is to solve Schrödinger's equation and Poisson's equation self-consistently [25:777; 82; 94]. The details of this method is beyond the scope of this thesis. This calculation has been performed numerically by Masselink [58] for $Al_xGa_{1-x}As/GaAs$ MODFETs and by Jaffe [44] for $In_yGa_{1-y}As/Al_xGa_{1-x}As$ MODFETs. The basics of the models reported in the literature will be described. Lee et al. developed an analytic model to calculate the 2DEG density (n_s) in modulation-doped heterostructures as a function of the doping density (N_D) in the $Al_xGa_{1-x}As$, the thickness of the undoped $Al_xGa_{1-x}As$ separation layer (d_1), the lattice temperature, and other device parameters [51]. The results of the proposed model show that the depletion approximation is not accurate enough and that Fermi-Dirac statistics (rather than Maxwell-Boltzmann statistics) should be used in the

calculation [51:2093]. To obtain a closed form solution, Lee et al. used the analytical approximation that the relationship between n_s and E_F is linear in the quantum well. The relationship is valid for $n_s > 5 \times 10^{11}$ cm^{-2} [25:782] and is given by [25:778; 51:2095]

$$q\Delta E_{F1} = q\Delta E_{F0}(T) + qan_s \quad \text{(eV)} \tag{2.2}$$

where

$q\Delta E_{F1}$ = the energy difference between the Fermi level and the bottom of the quantum well at the $Al_xGa_{1-x}As/GaAs$ heterointerface (see Fig. 2.6) (eV)

$a = 0.125 \times 10^{-12}$ (volt-cm^2)

$q\Delta E_{F0}$ = 0 (eV), at 300 °K

= 0.025 (eV), at 77 °K and below

Using (2.2), Lee et al. [28; 51; 96] showed that the thermal equilibrium 2DEG density n_{so} is determined by the $Al_xGa_{1-x}As$ parameters N_D, ε_2, and d_1 in the equation [51:2095; 96:1855]

$$n_{so} = \left\{ \frac{2\varepsilon_2 N_D[\blacktriangle E_c - q\Delta E_{F0}(T) + q\Delta E_{F2} + q\delta]}{q^2} + N_D^2(d_1 + \Delta d)^2 \right\}^{1/2} - N_D(d_1 + \Delta d) \tag{2.3}$$

where

q = electronic charge (1.602×10^{-19} Coul)

ε_2 = permittivity in the $Al_xGa_{1-x}As$ (F/cm)

$\blacktriangle E_c$ = conduction band-edge discontinuity (eV)

$q\Delta E_{F2}$ = $Al_xGa_{1-x}As$ equilibrium Fermi level, measured with respect to the conduction band edges (eV)

δ = a small voltage (e.g. a correction factor that depends on the donor level degeneracy factor, temperature, and N_D in the $Al_xGa_{1-x}As$ (volts)

$\Delta d = \epsilon_2 a/q$ (about 80 Å) is the effective position of the 2DEG (in the GaAs) from the heterointerface [28] (Å)

Expressions for ΔE_{F2} and δ are given in [51]. The analytic solution of (2.3) is compared to an exact numerical calculation in Fig. 2.8 with the undoped $Al_{0.3}Ga_{0.7}As$ layer thickness d_1 as a parameter. A more detailed model that accounts for shallow and deep donors in AlGaAs has been used to calculate the equilibrium 2DEG density of normal MODFETs [84].

Yoshida developed four one-dimensional numerical models to investigate the quantum mechanical effect on charge control in MODFETs [98]. A self-consistent quantum mechanical model was used to calculate the conduction band diagram and sub-band energy levels of a MODFET. The MODFET had a 300 Å $Al_{0.30}Ga_{0.7}As$ donor layer doped to 3×10^{18} cm^{-3}. No separation layer was used, and the gate voltage V_G was set to zero. The GaAs channel layer was assumed to have a background acceptor density of 1×10^{14} cm^{-3} and ΔE_c was assumed equal to $0.85\Delta E_g$. The result is shown in Fig. 2.9. The first two sub-bands, E_0 and E_1, contain over 85 percent of the channel electrons and are within about 100 Å of the heterointerface. Vinter has pointed out that sub-bands are also formed in the $Al_xGa_{1-x}As$ donor layer [94].

The maximum intrinsic transconductance and the maximum gate voltage swing for MODFETs are related to the equilibrium density of the 2DEG. These facts are discussed in the section on MODFET Device Modelling.

Mobility Enhancement. The prototype structure for modulation doping was the modulation-doped superlattice. Enhanced mobility in modulation-doped $Al_xGa_{1-x}As$/GaAs superlattices due to the absence of impurity scattering was first reported by Dingle et al.

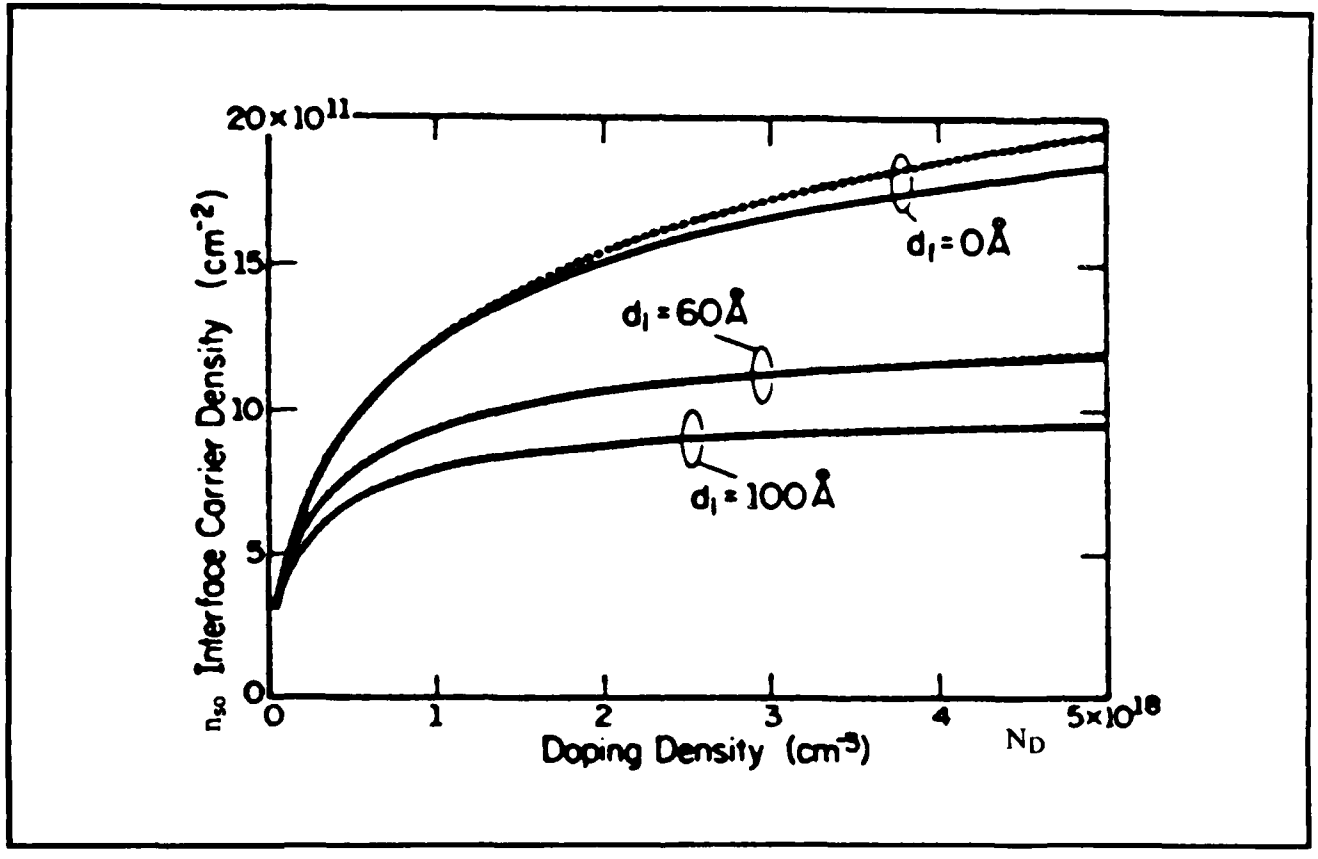

Fig. 2.8 Equilibrium 2DEG Density (n_{s0}) vs. $Al_{0.3}Ga_{0.7}As$ Doping Density with the Undoped $Al_{0.3}Ga_{0.7}As$ Separation Layer Thickness as a Parameter. Dotted Line: Numerical Solution; Solid Line: Determined from (2.3) above [51:2095]

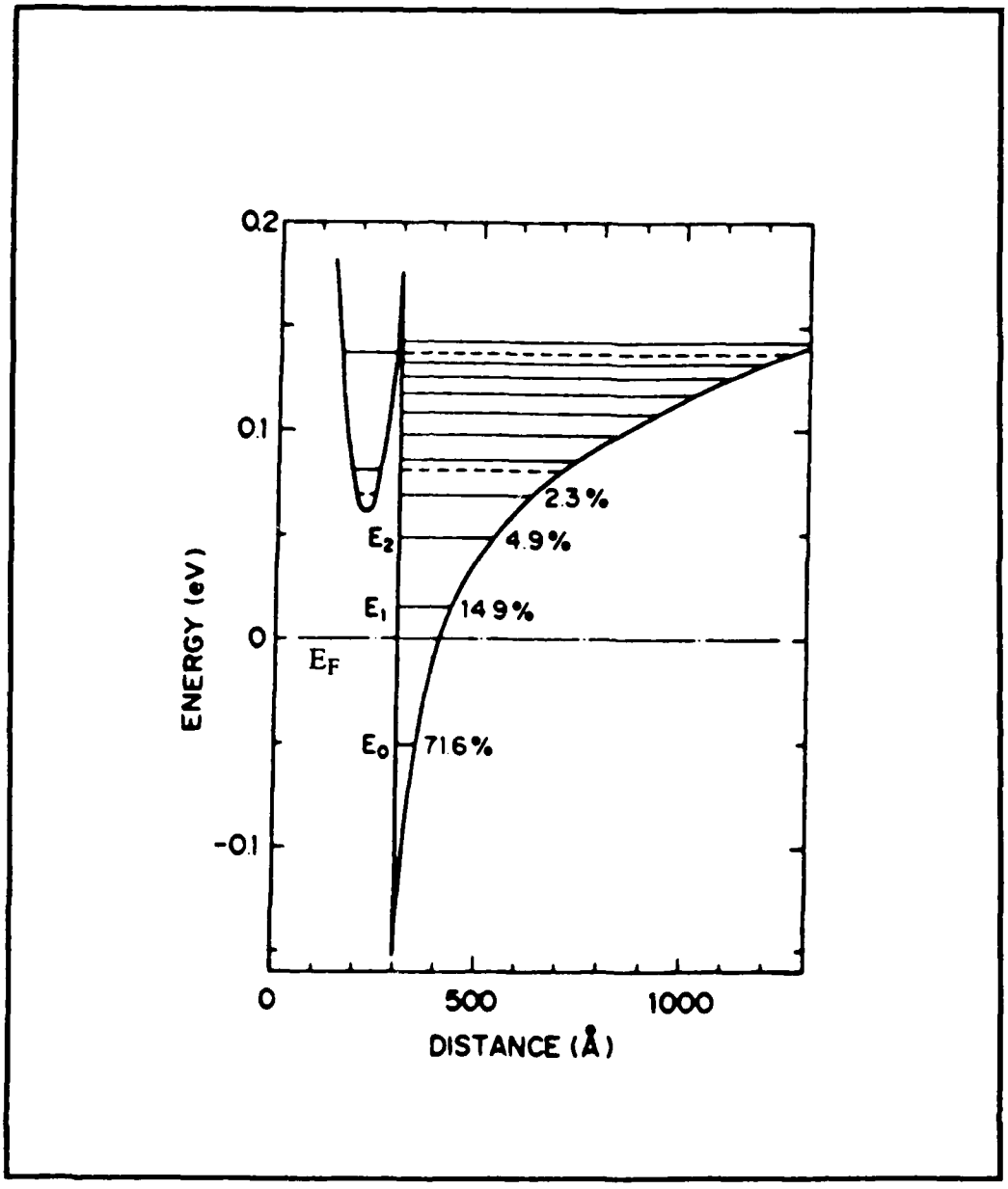

Fig. 2.9 Conduction Band-Edge and Sub-band Energy Levels of a MODFET. The Numerals in the Figure Indicate the Percent Occupations of the Sub-bands [98:155]

[22]. The energy band diagram of a multiple period $Al_xGa_{1-x}As/GaAs$ heterojunction structure (called a superlattice) is shown in Fig. 2.10. A modulation-doped superlattice is formed by doping the $Al_xGa_{1-x}As$ layers with silicon to facilitate the formation of free electrons. The GaAs layers are not doped, to allow maximum electron mobility. Figure 2.11 shows the measured low-field mobility parallel to the multilayers of a superlattice as a function of temperature. The modulation-doped superlattice structure has a substantially higher low-field mobility than that of bulk silicon-doped GaAs.

Drummond et al. have conducted mobility studies on single and multiple-period $Al_{0.33}Ga_{0.67}As/GaAs$ modulation-doped heterostructures (MDHs) that included separation layers of varying thicknesses [24; 26]. The $Al_{0.33}Ga_{0.67}As$ layers were doped with silicon to 7×10^{17} cm^{-3}. Plots of electron mobility vs. separation layer thickness d_1 at 300, 77, and 10 °K, and mobility vs.temperature for single period MDHs may be found in [24; 26]. Currently, repeatable Hall mobilities of 7×10^3 and 6×10^4 $cm^2/V\text{-}s$ at 300 and 77 °K, respectively, have been obtained for the MPD-H503 MODFET [87:109].

As discussed in [89:27-30, 44-49], the electron drift velocity (υ_n) in a semiconductor is proportional to the applied electric field (E). Thus $\upsilon_n = -\mu_n E$, where the proportionality constant is called the low-field electron mobility [90:32]. At large electric fields, the drift velocity approaches a saturation velocity (υ_s). In n-type GaAs, the drift velocity reaches a maximum, then decreases as E increases. This is due to the transfer of conduction electrons from a high mobility energy minimum valley ($\mu \approx 4000$ to 8000 $cm^2/V\text{-}s$) at the Brillouin zone center, to a low mobility (higher energy) satellite valley ($\mu \approx 100$ $cm^2/V\text{-}s$) along the <111> axes. The result is a differential negative mobility in GaAs for fields above 3×10^3 V/cm [89: 44-45]. Since MODFETs operate at high fields ($> 5 \times 10^3$ V/cm [25:780]), an understanding of field-dependent transport properties is required to accurately predict device behavior. The following section explores MODFET device characteristics and models. It will be shown that both the MODFET transconductance (g_m) and maximum

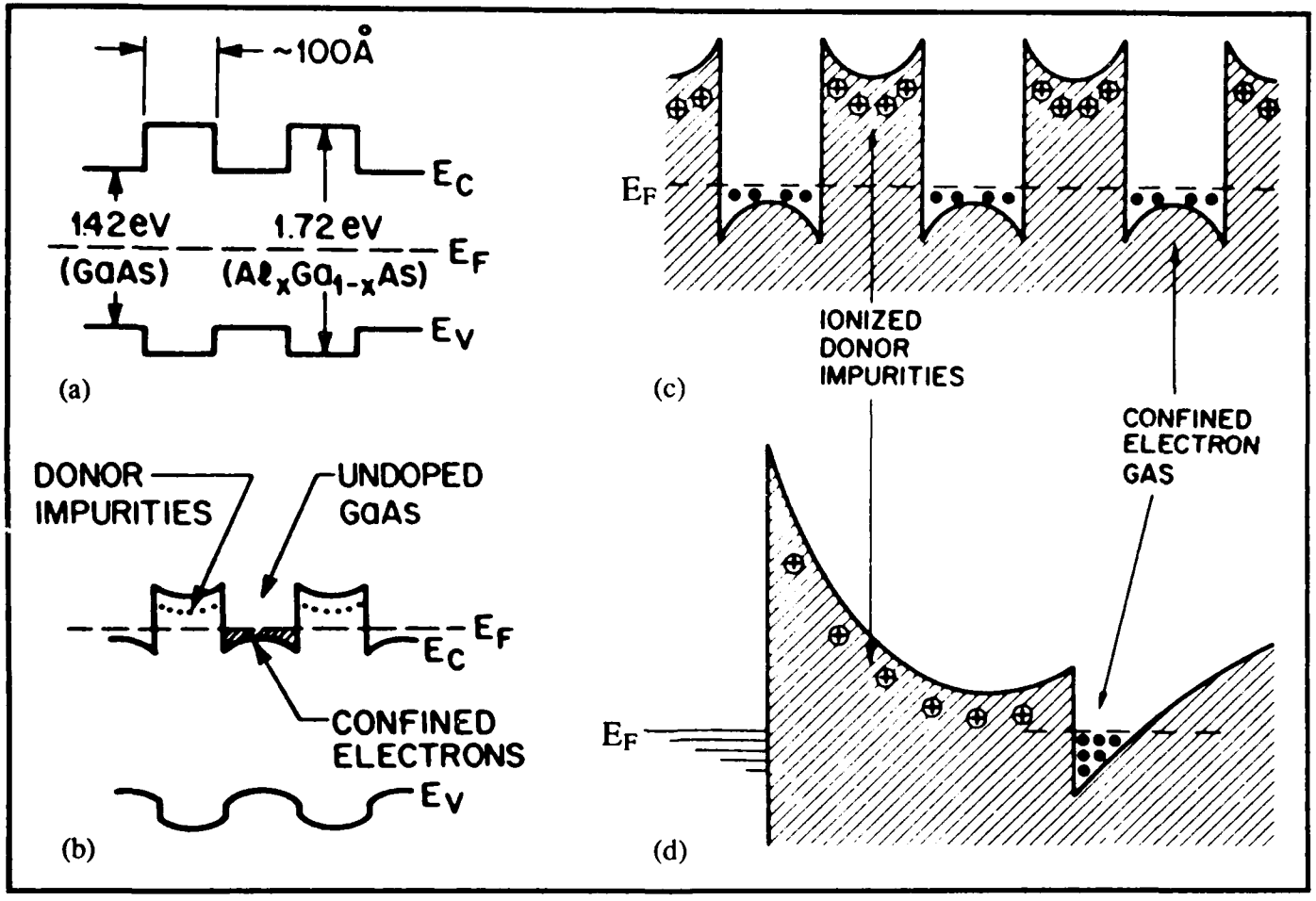

Fig. 2.10 Energy Band Diagrams for: (a) an Undoped Superlattice Structure; (b) and (c), a Modulation-Doped Superlattice Heterostructure (MDSH) and; (d) a One-Period MDSH with an Attached Schottky-Barrier Gate [45; 89: 128]

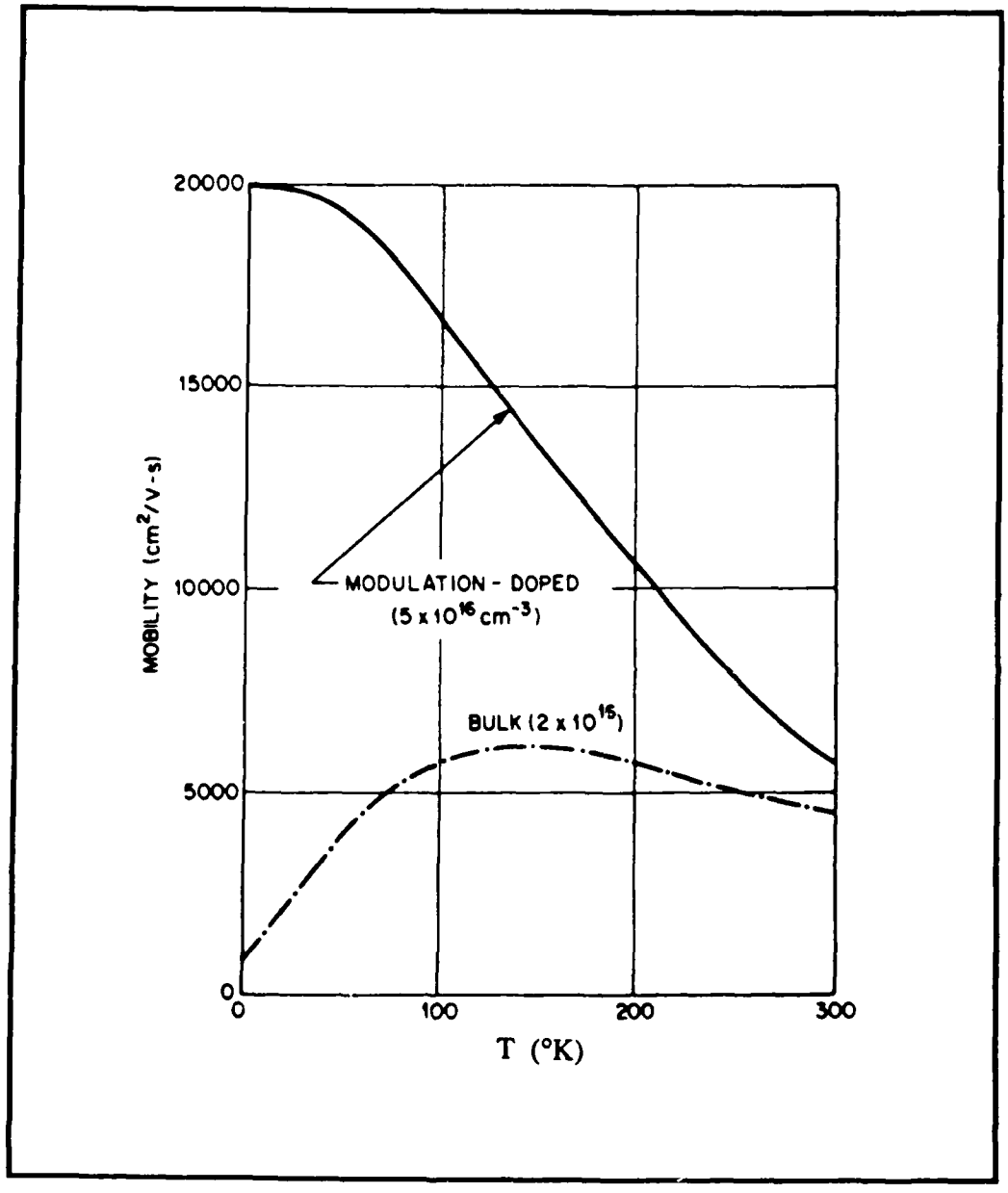

Fig. 2.11 Mobility vs. Temperature for Bulk GaAs and a Modulation-Doped Superlattice Structure [89:128]

forward current gain frequency (f_T) are directly related to the saturation velocity in the 2DEG channel.

MODFET Device Modelling

Several models for the MODFET have been reported [17; 20; 25; 28; 37; 57; 68; 95; 96]. The intent of this section is to give an overview of the MODFET models reported in the literature. It is expected that after slight modification, the models will be directly applicable to the MODFET devices fabricated in this study. This section is divided into three parts including: charge-control, MODFET I-V models, and MODFET microwave models.

Charge-Control. In a MODFET, the applied Schottky-barrier gate voltage (V_G) controls the number of electrons in the 2DEG channel, and thus, the current that flows from source to drain. The conduction band diagram for a MODFET at thermal equilibrium is shown in Fig. 2.12. The charge in the n-doped $Al_xGa_{1-x}As$ is depleted at the heterojunction by electron diffusion into the GaAs. Charge is also depleted by the built-in voltage (ϕ_B) of the Schottky-barrier gate. To avoid conduction through the n-$Al_xGa_{1-x}As$ layer (e.g. a parasitic MESFET path), parameters must be chosen so that the two depletion regions overlap. In a depletion mode device, the depletion regions just touch (or slightly overlap) and the 2DEG forms with $V_G = 0$. This structure is used for analog applications such as microwave low-noise amplifiers. By recessing the gate (e.g. decreasing the thickness of the n-$Al_xGa_{1-x}As$ layer) the gate's depletion region will eventually extend into the undoped GaAs layer and deplete the 2DEG with $V_G = 0$. The result is an enhancement mode or normally-off device. In this case, a voltage greater than the threshold voltage (V_{OFF}) must be applied to force the depletion region back into the doped $Al_xGa_{1-x}As$. This allows the 2DEG to form and the channel to conduct. This type of device is used in high-speed digital circuits. Increasing the AlAs mole fraction in the $Al_xGa_{1-x}As$ permits higher forward gate voltages on the device,

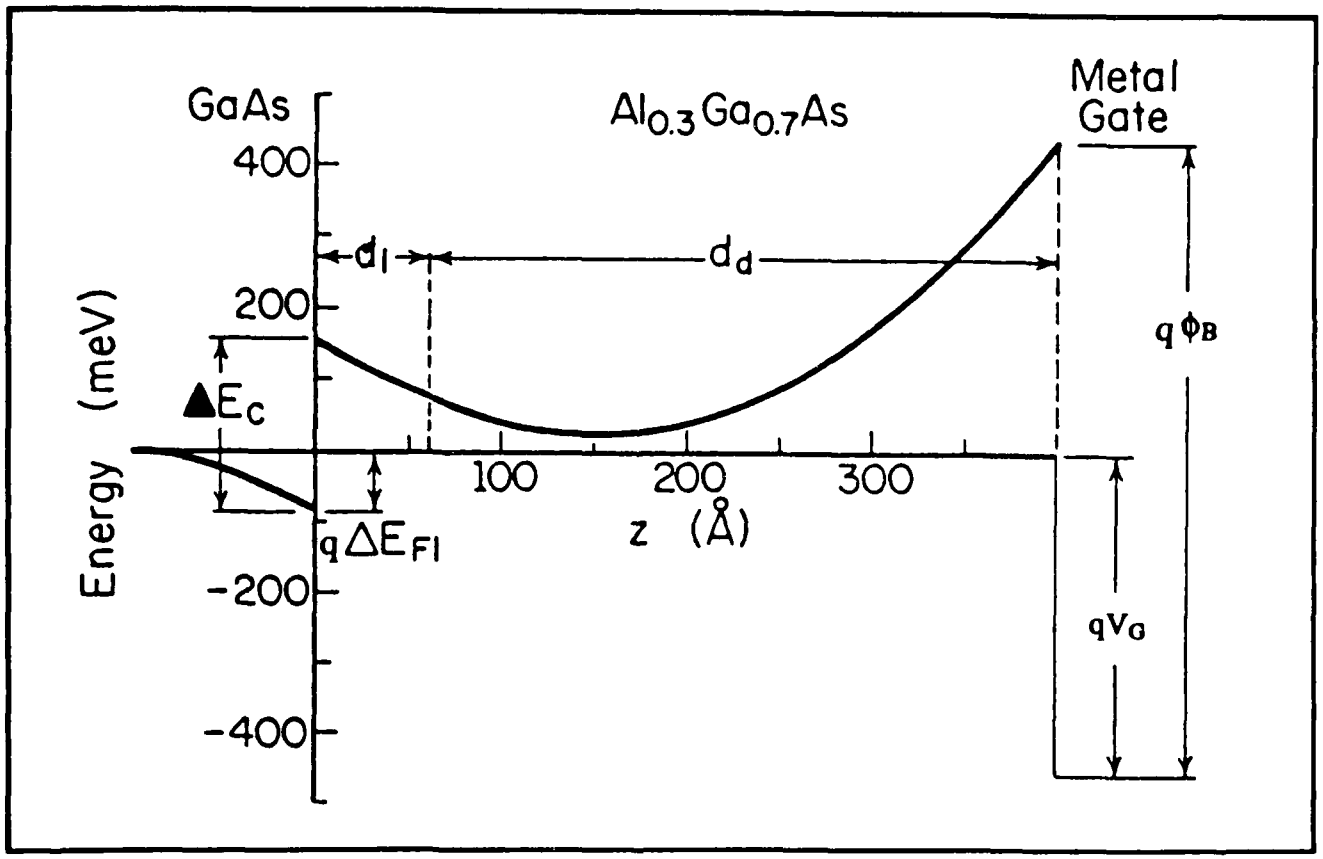

Fig. 2.12 Conduction Band Diagram for a MODFET with a Schottky-Barrier Gate [58]

reduces unwanted injection of "hot" carriers (thermionic electrons) from the GaAs into the $Al_xGa_{1-x}As$, and permits higher electron densities in the 2DEG channel without parasitic conduction in the n-$Al_xGa_{1-x}As$ [65:32]. Maximum voltages on the gate are limited. Too high a gate voltage causes current leakage at the Schottky-barrier gate and conduction in the n-$Al_xGa_{1-x}As$ layer. Applied gate voltages are limited to about 0.8 V unless, for example, a p^+-GaAs surface layer is added under the gate [70].

The first step in modelling the behavior of a MODFET is to obtain a solution to the one-dimensional problem of charge control by an electrical gate [25:781]. A model for charge transfer across a modulation-doped heterojunction was first reported by Delagebeaudeuf and Linh [21] and later improved by Lee et al. [51]. The expression presented below for MODFET charge-control was developed by Drummond et al. [25:782; 28]. Referring to Fig. 2.13, the density of electrons n_s (cm^{-2}) in the 2DEG depends on the applied gate voltage V_G according to the following equation [25:778]:

$$\begin{aligned} n_s &= \frac{\varepsilon_2}{q(d + \Delta d)}(V_G - V_{OFF}) \quad (cm^{-2}) \quad (V_G > V_{OFF}) \\ &= 0 \quad (cm^{-2}) \quad (V_G \le V_{OFF}) \end{aligned} \tag{2.4}$$

where

$d = d_d + d_1$ (Å)

d_d = thickness of n-$Al_xGa_{1-x}As$ (Å)

d_1 = thickness of undoped $Al_xGa_{1-x}As$ separation layer (Å)

$\Delta d = \varepsilon_2 a/q$ (Å)

V_G = applied gate voltage (volts)

$V_{OFF} = \phi_B - qN_D{}^2 d_d/\varepsilon_2 - \Delta E_c + \Delta E_{F0}$ (threshold voltage) (volts)

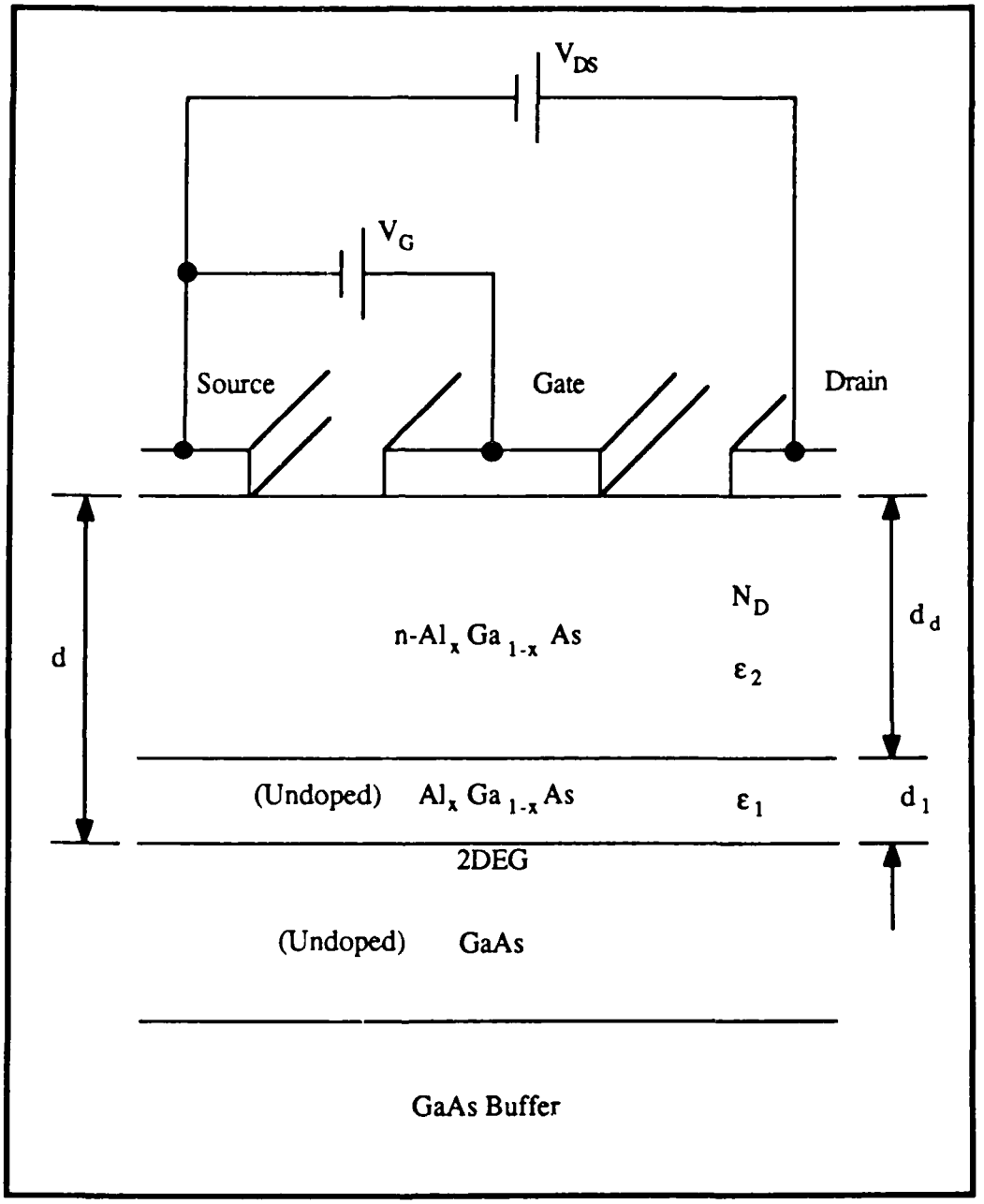

Fig. 2.13 MODFET Dimensions for the Charge-Control Equation

The charge-control equations that are derived in Appendices A and B have the form of (2.4).

MODFET I-V Models. A model for the MODFET channel charge density and current, as a function of the gate and drain voltages, was first developed by Delagebeaudeuf and Linh (as for charge-control above) [21]. Lee et al. [28; 51] advanced this model to include the variation of the Fermi energy level with the 2DEG density. Lee et al. used a linearized $\Delta E_{F1}(n_S)$ dependence (see (2.2)), and two- and three-piece models of the electron velocity-field dependence, to model the MODFET I-V characteristics. Their model is valid only for gate voltages below which there is no parallel conduction in the $Al_xGa_{1-x}As$ layers. Another group [96] then reported on a MODFET I-V (and microwave) model that uses an analytic velocity vs. electric field model, and a numerical integration to obtain V_{DS} for a given V_{GS} and I_{DS}.

Two closed-form I-V models for MODFETs were recently developed [37; 68]. The first model [37] uses fitting parameters from an empirical expression for velocity vs. electric field and for drain conductance in the drain current saturation region. According to its authors, this model is a promising candidate for implementation on a circuit simulator such as SPICE. The second model [68] contains some of the parameters found in (2.4) and also includes MODFET source (R_S) and drain (R_D) resistance parameters. A final analytical model that is able to cover the entire operational range of the MODFET including the sub-threshold region was recently developed [95].

The transconductance (slope of the drain current vs. gate voltage characteristic) determines (in large part) both the DC and microwave performance of the MODFET [65:33]. The extrinsic transconductance is given by

$$g_m = \frac{\Delta I_D}{\Delta V_G Z} \qquad \text{(mS/mm)} \tag{2.5}$$

where Z is the gate width. The intrinsic transconductance (g_{mo}) may be written [36:289]

$$g_{mo} = \left(\frac{g_m}{1 - g_m R_S} \right) \quad \text{(mS)} \tag{2.6}$$

where R_s is the source resistance. The intrinsic transconductance of short gate-length FETs (about 1 μm or less) operating in the velocity saturation mode is given by [4:1400]

$$g_{mo} = \frac{\varepsilon_s \upsilon_s Z}{d_{eff}} \quad \text{(mS)} \tag{2.7}$$

where

ε_s = permittivity of the material ($Al_xGa_{1-x}As$) in the depletion region (F/cm)

υ_s = electron saturation velocity in the channel (cm/s)

$d_{eff} = d_d + d_1 + \Delta d$ (Å)

Since d_{eff} is the thickness of the $Al_xGa_{1-x}As$ layer (plus Δd which is voltage dependent [63:1675]), decreasing d_{eff} results in a higher g_{mo}. However, decreasing d_{eff} will also decrease the 2DEG density unless the doping of the $Al_xGa_{1-x}As$ is increased.

Another important parameter in MODFETs is the gate-to-source capacitance (C_{gs}) [63:1675]. Under the short channel approximation [38:601]

$$g_{mo} = \frac{C_{gs} \upsilon_s}{L_G} \quad \text{(mS)} \tag{2.8}$$

where L_G is the gate-length (μm). By substituting (2.8) into (2.7), the gate-to-source capacitance becomes

$$C_{gs} = \frac{\varepsilon_s L_G Z}{d_{eff}} \quad \text{(pF)} \tag{2.9}$$

MODFET Microwave Models. A small-signal equivalent circuit model used to model MODFETs is shown in Fig. 2.14. Typically, the MODFET's (2-port) scattering parameters (S-parameters) are first measured and then admittance and hybrid parameters (y-parameters and h-parameters, respectively) may be computed. The equivalent circuit parameters may be determined by using computer analysis software such as Super-Compact PC [35:649; 85] or Touchstone [92].

The S-parameters (S_{11}, S_{12}, S_{21}, S_{22}) may also be used to calculate the maximum power gain (G_{max}) and the forward current gain (h_{21}) of the MODFET. The following equations are used to calculate G_{max} [52:121] and h_{21} [33:24]:

$$G_{max} = \frac{|S_{11}|}{|S_{12}|}\left|K \pm (K^2 - 1)^{1/2}\right| \quad \text{(unitless)} \qquad (2.10a)$$

where

$$K = \frac{1 + |S_{11}S_{22} - S_{12}S_{21}|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{12}S_{21}|} \quad \text{(unitless)} \qquad (2.10b)$$

and

$$h_{21} = \frac{-2S_{21}}{(1 - S_{11})(1 + S_{22}) - S_{12}S_{21}} \quad \text{(unitless)} \qquad (2.11)$$

A widely used figure of merit for microwave amplifiers is the maximum (or unity) forward current gain frequency (f_T). For the MODFET [38:602]

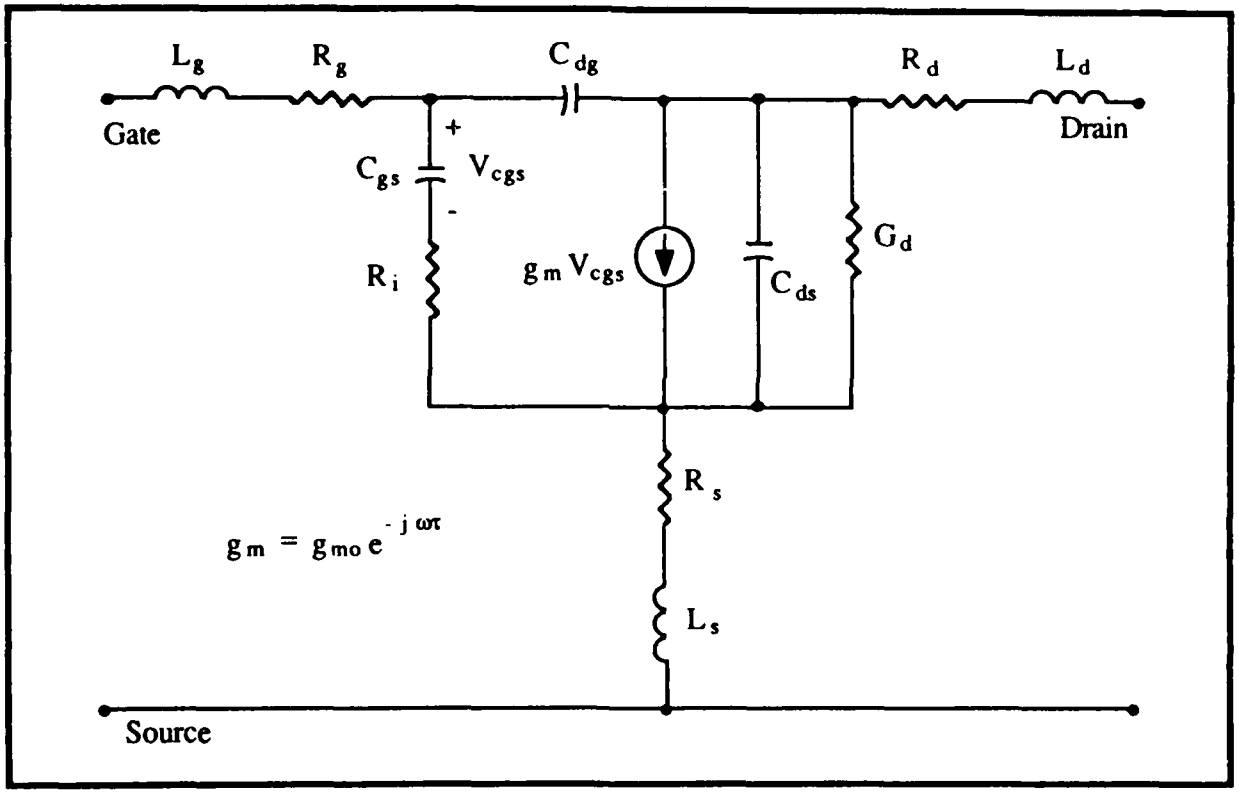

Fig. 2.14 Small-Signal Equivalent Circuit Model for the MODFET [35:650]

$$f_T = \frac{g_{mo}}{2\pi C_{gs}} = \frac{\upsilon_{avg}}{2\pi L_G} = \frac{1}{2\pi\tau} \quad \text{(GHz)} \qquad (2.12)$$

where τ is the average transit time for an electron to travel through the channel and υ_{avg} is the average electron velocity (υ_s at high electric fields) under the gate. The maximum forward current gain frequency is given by (2.11) when $|h_{21}| = 1$ (0 dB). Another figure of merit, the maximum frequency of oscillation (f_{max}), is given by (2.10) when $|G_{max}| = 1$ (0 dB). The term f_{max} is given by [4:1400]

$$f_{max} = \frac{f_T}{\{2[(R_i + R_g + R_s)G_d + 2\pi f_T R_g C_{dg}]^{1/2}\}} \quad \text{(GHz)} \qquad (2.13)$$

A final figure of merit is the noise figure (NF). The NF is described by the following empirical equation [38:601]:

$$NF = 1 + \kappa\frac{f}{f_T}[g_{mo}(R_s + R_g)]^{1/2} \quad \text{(unitless)} \qquad (2.14)$$

where f is the operating frequency (GHz) and κ is a fitting factor. Substituting (2.8), (2.9), and (2.12) into (2.14) yields

$$NF = 1 + 2\pi\kappa f\left[\frac{\varepsilon_s L_G^2 Z(R_s + R_g)}{d_{eff}\upsilon_s}\right]^{1/2} \quad \text{(unitless)} \qquad (2.15)$$

Equation (2.15) implies that an increase in the AlGaAs layer thickness (d_{eff}), a decrease in the parasitic source or gate resistance, or a decrease in gate length will lead to a lower noise figure when all other parameters remain constant. Thus a trade-off between transconductance and noise figure exists.

Enhanced Schottky-Barrier MODFETs

The enhanced Schottky-barrier (ES)MODFET is a normal MODFET with the addition of a thin p^+-GaAs layer under the gate. The purpose of the added layer is to increase the effective Schottky-barrier height, and thus increase the allowable applied gate voltage. Too large a gate voltage results in excessive gate leakage current (through tunneling, thermionic emission, and other transport mechanisms) and lowers the device's noise margin [53].

Schottky-Barrier Enhancement. In standard Schottky barriers, the barrier height is primarily determined by the character of the metal and the metal-semiconductor interface property and is nearly independent of the doping [89:293]. Therefore, a finite number of choices for barrier height (ϕ_B) exist for a given semiconductor. However, Shannon [77] has shown that the effective barrier height for a given metal-semiconductor contact can be varied by introducing a thin layer (about 100 Å or less) of semiconductor with a controllable number of dopants between the metal-semiconductor interface. Figure 2.15 illustrates the idealized controlled Schottky-barrier contacts with a thin n^+-layer (barrier reduction) or a thin p^+-layer (barrier raising) on an n-type substrate. For the case of a p^+-layer, the potential at the metal/p^+-layer interface will be $q\phi_B$ (eV) at $z = 0$ [89:295] and will reach a maximum at $z = \Delta$, where

$$\Delta = \frac{1}{p_1}[ap_1 - (W - a)n_2]$$

where

a = thickness of the p^+-layer (Å)

W = depletion region width (Å)

p_1 = doping density of the p^+-layer ($N_A - N_D$) (cm^{-3})

n_2 = doping density of the n-type substrate ($N_D - N_A$) (cm^{-3})

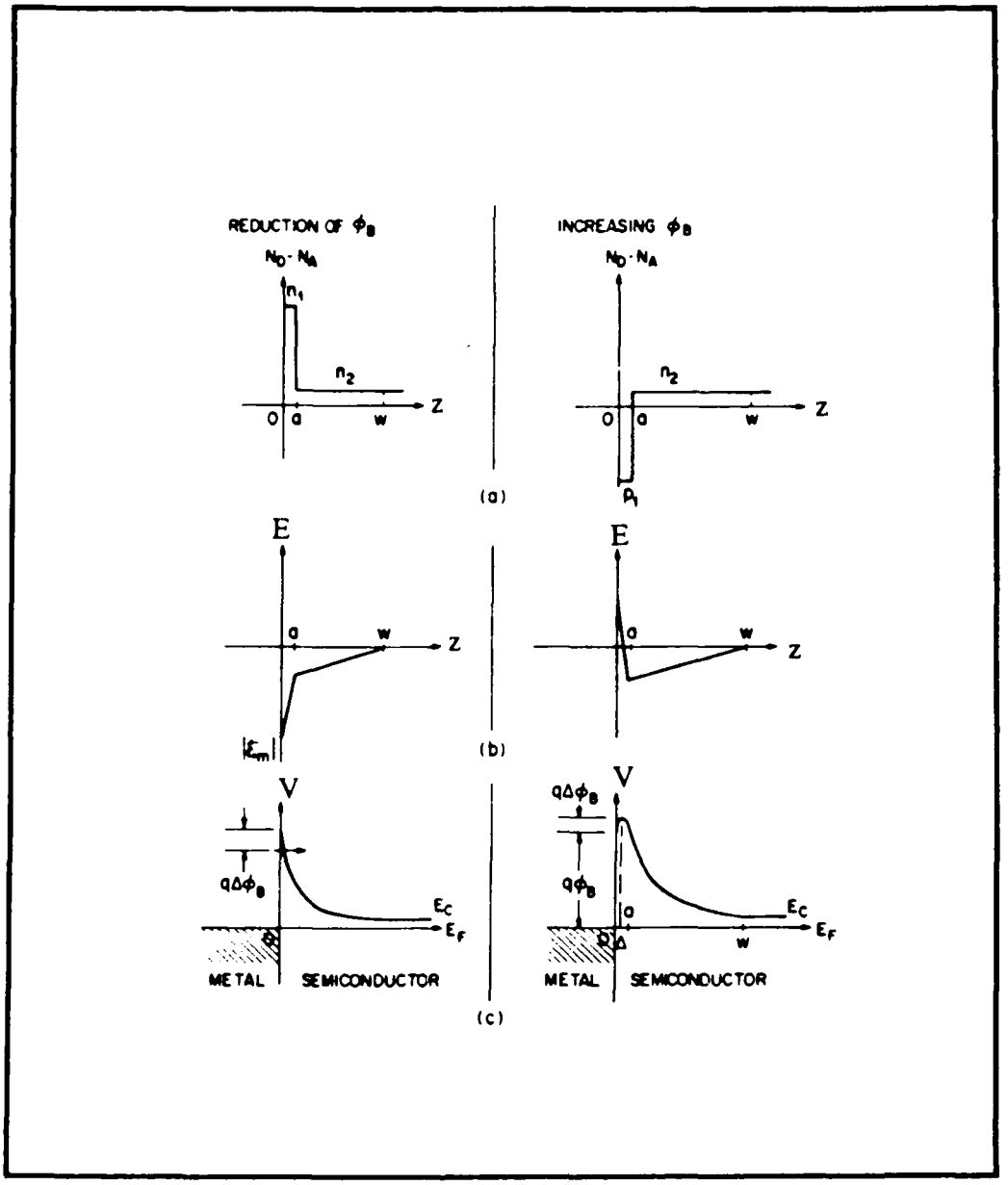

Fig. 2.15 Idealized Controlled Barrier Contacts with a Thin n^+-Layer or a Thin p^+- Layer on an n-Type Substrate for Barrier Reduction or Barrier Raising, Respectively [89:294]

The effective barrier height (ϕ_B*) (e.g. the largest potential barrier to electrons) occurs at $z = \Delta$ and is given by [89:295]

$$\phi_B^* = \phi_B + E_m\Delta - \frac{qp_1\Delta^2}{2\varepsilon_s}$$

where E_m is the maximum electric field and ε_s is the substrate's permittivity. The value of ϕ_B* approaches ($\phi_B + qp_1a^2/2\varepsilon_s$) if $p_1 >> n_2$ and $ap_1 >> n_2W$. Thus as the product (ap_1) increases, the effective barrier height will also increase.

An analytic model for the barrier height enhancement of Schottky-barrier diodes may be found in [97]. The Camel gate FET, described in [91], also makes use of Schottky-barrier modification to improve device reliability and power handling capability. Recently, the concept of Schottky-barrier enhancement was applied to MODFETs [60; 70] and is expanded upon in the next sub-section.

Enhanced Schottky-Barrier MODFET Structure and Fabrication. The structure and conduction band diagram of the (ES)MODFET fabricated by Priddy et al. is shown in Fig. 2.16. The device has conduction band discontinuities (ΔE_c) at both the $Al_{0.3}Ga_{0.7}As$/GaAs and n-$Al_{0.3}Ga_{0.7}As$/p^+-GaAs heterointerfaces. The (ES)MODFET was fabricated identically as a normal MODFET except for the additional MBE-grown p^+-GaAs (beryllium-doped to 2×10^{19} cm^{-3}) epitaxial layer. Ohmic contacts (AuGe/Ni) alloyed through the p^+-GaAs layer and a Ti/Au gate were used. After the FET processing was completed, the p^+-GaAs cap layer was etched (with the metallization pattern as a mask) between the gate and drain, and the gate and source, by placing the entire wafer in a selective etchant (pH adjusted $NH_4OH:H_2O_2$) [70:177]. The forward gate turn-on voltage of the (ES)MODFET was shown to be as high as 1.6 Volts (compared to 0.8 Volts for the normal MODFET). A similar device with a p^+-GaAs surface layer and graded

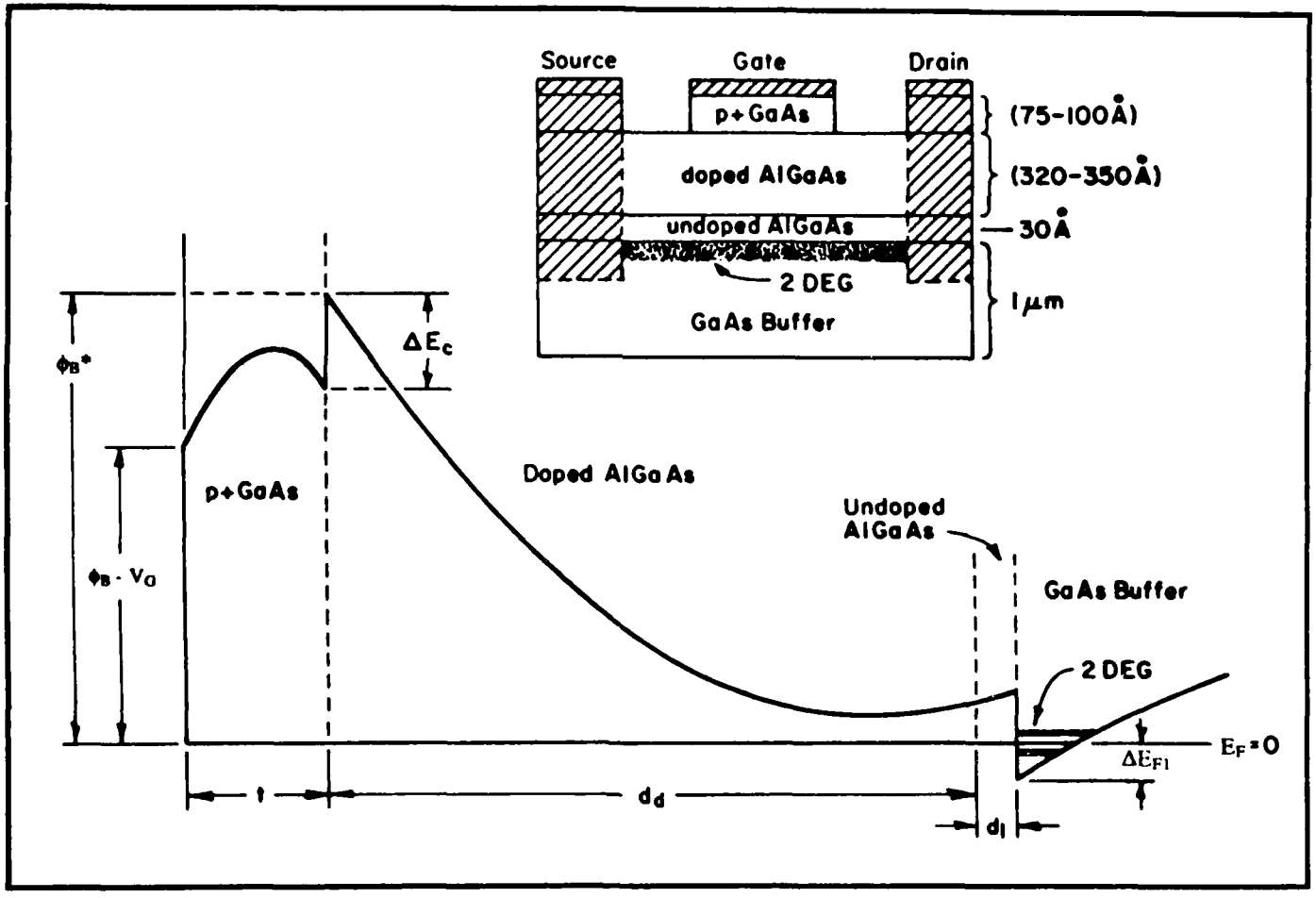

Fig. 2.16 (a) Structure and (b) Conduction Band Diagram of an ESMODFET [70:175]

n-$Al_xGa_{1-x}As$ barrier layer has been fabricated by Ohata et al. [67]. Grading the n-$Al_xGa_{1-x}As$ layer from x = 0.3 to 0 removed the conduction band notch (ΔE_c) at the p^+-GaAs/n-$Al_xGa_{1-x}As$ heterointerface and is a technique that has been used to improve the performance of heterojunction bipolar transistors [11].

Pseudomorphic MODFETs

Pseudomorphic MODFETs are based on an $In_yGa_{1-y}As/Al_xGa_{1-x}As$ modulation-doped heterostructure. Also called a strained channel MODFET [44], this device has important advantages over the more widely studied $Al_xGa_{1-x}As$/GaAs system.

Pseudomorphic MODFET Structure and Fabrication. The structure and associated conduction band diagram of a single-quantum-well $In_yGa_{1-y}As/Al_xGa_{1-x}As$ MODFET is shown in Fig. 2.17. The structure is grown by MBE and is essentially the same as a normal $Al_xGa_{1-x}As$/GaAs MODFET except for one of the epitaxial layers. An undoped $In_{0.15}Ga_{0.85}As$ quantum-well layer is interposed between the 1 μm GaAs buffer layer and the 30 Å $Al_{0.15}Ga_{0.85}As$ separation layer. The 2DEG is now confined in this $In_{0.15}Ga_{0.85}As$ layer. The n-$Al_{0.15}Ga_{0.85}As$ is Si-doped to 3×10^{18} cm^{-3}.

A lattice constant mismatch (Δa) of about 1 percent exists between the GaAs buffer layer and the $In_{0.15}Ga_{0.85}As$ strained channel layer. A similar lattice constant mismatch exists at the $In_{0.15}Ga_{0.85}As/Al_{0.15}Ga_{0.85}As$ heterointerface. In order to match the lattice constants of GaAs and $Al_xGa_{1-x}As$, the $In_{0.15}Ga_{0.85}As$ layer undergoes a tetragonal distortion (compression) from its normal cubic crystalline structure (the epitaxial lattice planes normal to the substrate elongate). The $In_{0.15}Ga_{0.85}As$ is compressed (strained) along the direction parallel to the heterointerface in order to mirror the morphology or structure of the GaAs (and the structure of the $Al_{0.15}Ga_{0.85}As$) and is termed a "pseudomorphic" layer [46]. The lattice mismatch induced strain between the $In_yGa_{1-y}As$ and the GaAs (and $Al_xGa_{1-x}As$) can be entirely accommodated elastically if the $In_yGa_{1-y}As$ epitaxial layer is at or below a

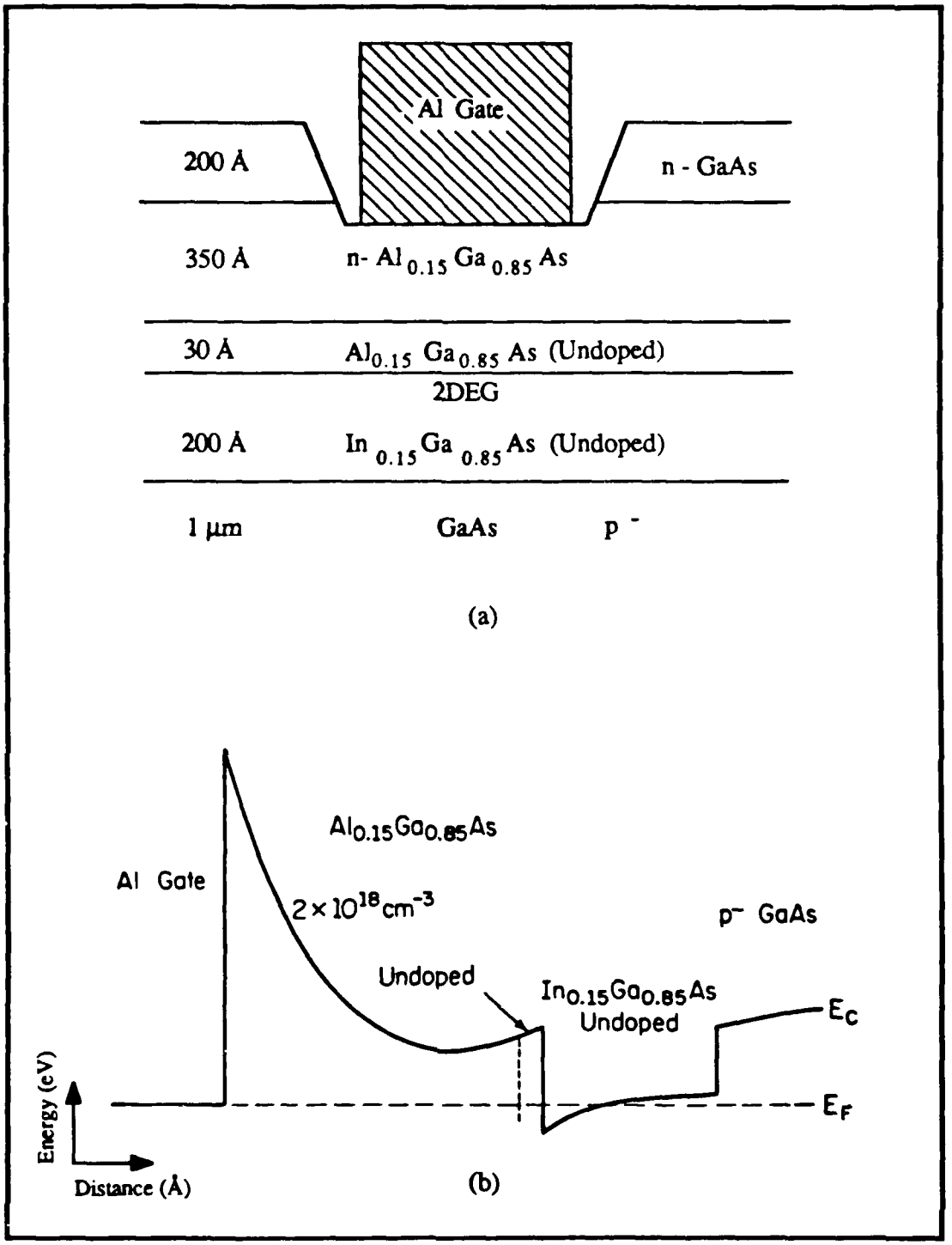

Fig. 2.17 (a) Structure and (b) Conduction Band Diagram for an InGaAs/AlGaAs Pseudomorphic MODFET [46:629]

critical thickness, according to a theory developed by Matthews and Blakeslee [59] (this is called commensurate epitaxy). The dependence of critical thickness on the InAs mole fraction (y) is shown in Fig. 2.18. For $y = 0.15$, the $In_{0.15}Ga_{0.85}As$ epitaxial layer thickness must not exceed about 200 Å, which dictates the epitaxial layer structure of the pseudomorphic MODFET.

The electron saturation velocity (υ_s) and low-field mobility (μ_n) in bulk $In_yGa_{1-y}As$ is expected to increase with increasing InAs mole fraction [36:288]. The υ_s of $In_{0.53}Ga_{0.47}As$ has been determined to be 2.85×10^7 cm/s, which is 33 percent larger than the υ_s of GaAs, about 2.13×10^7 cm/s [88:140]. However, attempts to grow smooth pseudomorphic epitaxial layers for $y > 0.3$ have been generally unsuccessful (e.g. at $y = 0.53$, a layer thickness less than 35 Å is required) [88:140]. Henderson et al. have shown that above a certain InAs mole fraction (about 0.13 at 77 °K), strain begins to degrade transport properties within pseudomorphic $In_yGa_{1-y}As$ quantum-well structures [36:290].

The fabrication of individual MODFETs on pseudomorphic MBE-grown wafers is identical to the process used for normal MODFETs and was described earlier. Appendix D contains the pseudomorphic MODFET fabrication process used in this study.

Advantages of Pseudomorphic MODFETs. Ketterson et al. [46; 47] have experimentally verified the theoretical advantages of $In_yGa_{1-y}As/Al_xGa_{1-x}As$ pseudomorphic MODFETs compared to devices based on the $Al_xGa_{1-x}As/GaAs$ system. First, in order to obtain a 2DEG concentration on the order of 10^{12} cm^{-2}, a heterojunction conduction band discontinuity (ΔE_c) of about 0.3 eV is required. In general, increasing the AlAs mole fraction allows higher 2DEG channel concentrations without parasitic MESFET conduction in the n-$Al_xGa_{1-x}As$ layer and also reduces hot-electron injection into the higher bandgap material [46:564]. In the $Al_xGa_{1-x}As/GaAs$ system, an AlAs mole fraction (x) greater than 0.2 is required [46:564]. In present practice, x varies between 0.25 - 0.3 [81:1022]. Since $In_yGa_{1-y}As$ has a smaller bandgap than GaAs, a mole fraction of

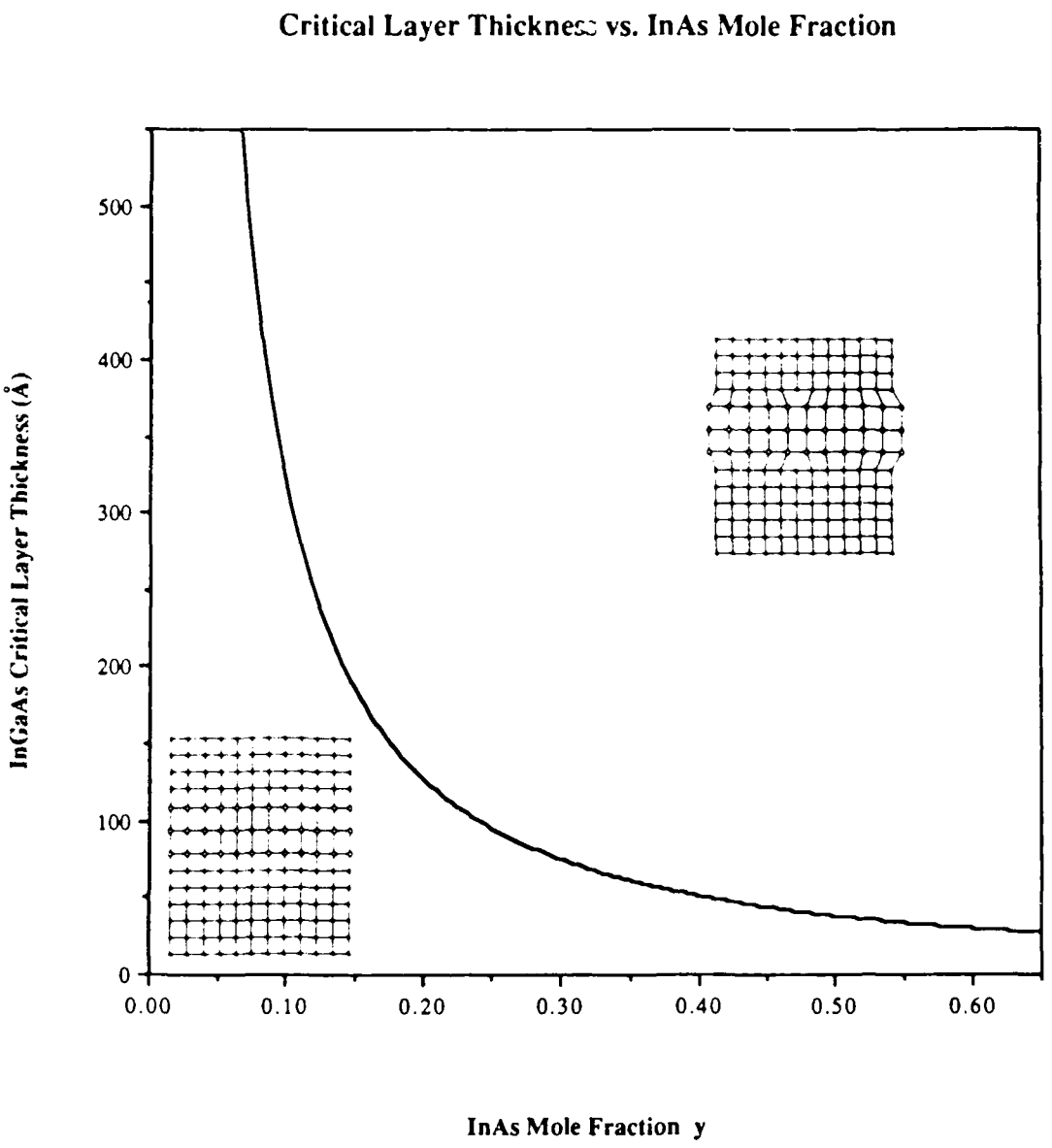

Fig. 2.18 Critical Layer Thickness vs. InAs Mole Fraction [88:140]

$x = 0.15$ is sufficient for a ΔE_c of about 0.3 eV [46:564]. However, modulation-doped structures with an AlAs mole fraction greater than 0.2 suffer from persistent photoconductivity (PPC) effects below 100 °K [65:35]. When exposed to light, MODFETs at low temperatures produce a photocurrent that decays over several days. The PPC effects result in "collapse" of drain I-V characteristics (at low temperatures) if the n-$Al_xGa_{1-x}As$ is not grown under optimum conditions [31; 46:564]. Deep level donor related defects (traps) called D-X centers in the n-$Al_xGa_{1-x}As$ are believed to be the cause of the PPC effects [25:795]. Additionally, MODFETs with an $Al_xGa_{1-x}As$ layer where $x \geq 0.25$ suffer from a high density of defects that lead to extremely high low-frequency noise, generation-recombination noise, large resistances (within device models), and related degraded performance [54]. Thus, the $In_{0.15}Ga_{0.85}As$/ $Al_{0.15}Ga_{0.85}As$ pseudomorphic MODFET maintains a large ΔE_c while simultaneously reducing the D-X center occupation probability and related device noise [50].

A second advantage of the pseudomorphic MODFET is its higher saturation velocity υ_s. A higher υ_s leads to higher intrinsic transconductances (g_{mo}). Also, higher doping densities are possible with low mole fraction $Al_xGa_{1-x}As$ due to reduced donor compensation [47:628]. This reduces the required n-$Al_xGa_{1-x}As$ layer thickness and lowers parasitic source (R_s) and drain (R_d) resistances (e.g. minimizing the semiconductor sheet conductivity between contact terminals [25:793]). The parameters R_s and R_d are important for overall MODFET performance. Finally, the limiting forward current gain frequency (f_T) in a short channel MODFET (or MESFET) is given by $f_T = \upsilon_{avg}/2\pi L_G$ (see (2.12)). Thus a large υ_s results likewise in a correspondingly large f_T, which in turn (from (2.13)) leads to a large maximum frequency of oscillation (f_{max}). A pseudomorphic MODFET with a gate length of 0.25 μm and a gate width of 50 μm was recently shown to have an f_{max} equal to 230 GHz [88:142].

The $In_{0.15}Ga_{0.85}As$ quantum-well layer has energy barriers of 0.3 eV on the $Al_{0.15}Ga_{0.85}As$ side and 0.17 eV on the GaAs side (forming a quasi-rectangular quantum-well) [54:577]. In the normal MODFET, the 2DEG is confined by the ΔE_c of the $Al_xGa_{1-x}As$/GaAs on one side, and the electric field due to electron accumulation on the other side. The ΔE_c and electrostatic confinement forces are also present in the pseudomorphic MODFET. The second conduction band discontinuity of 0.17 eV provides additional 2DEG confinement, and results in a lower output conductance and a greater power added efficiency for the device [88:146].

Transport Characteristics. The measured transport characteristics for the pseudomorphic MODFET fabricated by Ketterson et al. will now be presented. The electron mobilities and velocities vs. electric field at 77 and 300 °K are shown in Fig. 2.19(a) and (b), respectively. Hall measurements indicated a 300 °K low-field mobility and 2DEG areal concentration of 6000 cm^2/V-s and 1.4 x 10^{12} cm^{-2} respectively, (with no PPC effects) [46:565]. When the 30 Å $Al_{0.15}Ga_{0.85}As$ separation layer was replaced by a 100 Å thick layer, the 2DEG sheet density (n_s) decreased to 3 x 10^{11} cm^{-2}, and the Hall mobility increased to 8000, 95,000, and 158,000 cm^2/V-s at 300, 77, and 10 °K, respectively [46:565]. The latter value represents the highest mobility yet reported for a strained-layer MODFET. The electron velocities in the MODFET begin to saturate as the critical field (3 x 10^3 volts/cm) between the drain and source is approached as shown in Fig. 2.19(b). An electron velocity of 1.7 x 10^7 cm/s (with an n_s of 1.35 x 10^{12} cm^{-2}) was measured at an electric field strength of 3050 V/cm [46:566].

Pseudomorphic MODFET DC and Microwave Characteristics. The current-voltage (I-V) and transfer characteristics for the pseudomorphic MODFET (1 x 145 μm^2) structure of Fig. 2.17 are shown in Fig. 2.20. The threshold voltage (V_{OFF}), defined by a linear extrapolation of the drain current vs. gate voltage to zero current [46:566], is about - 0.3 volts. A peak transconductance of 270 mS/mm at 300 °K was measured at a gate

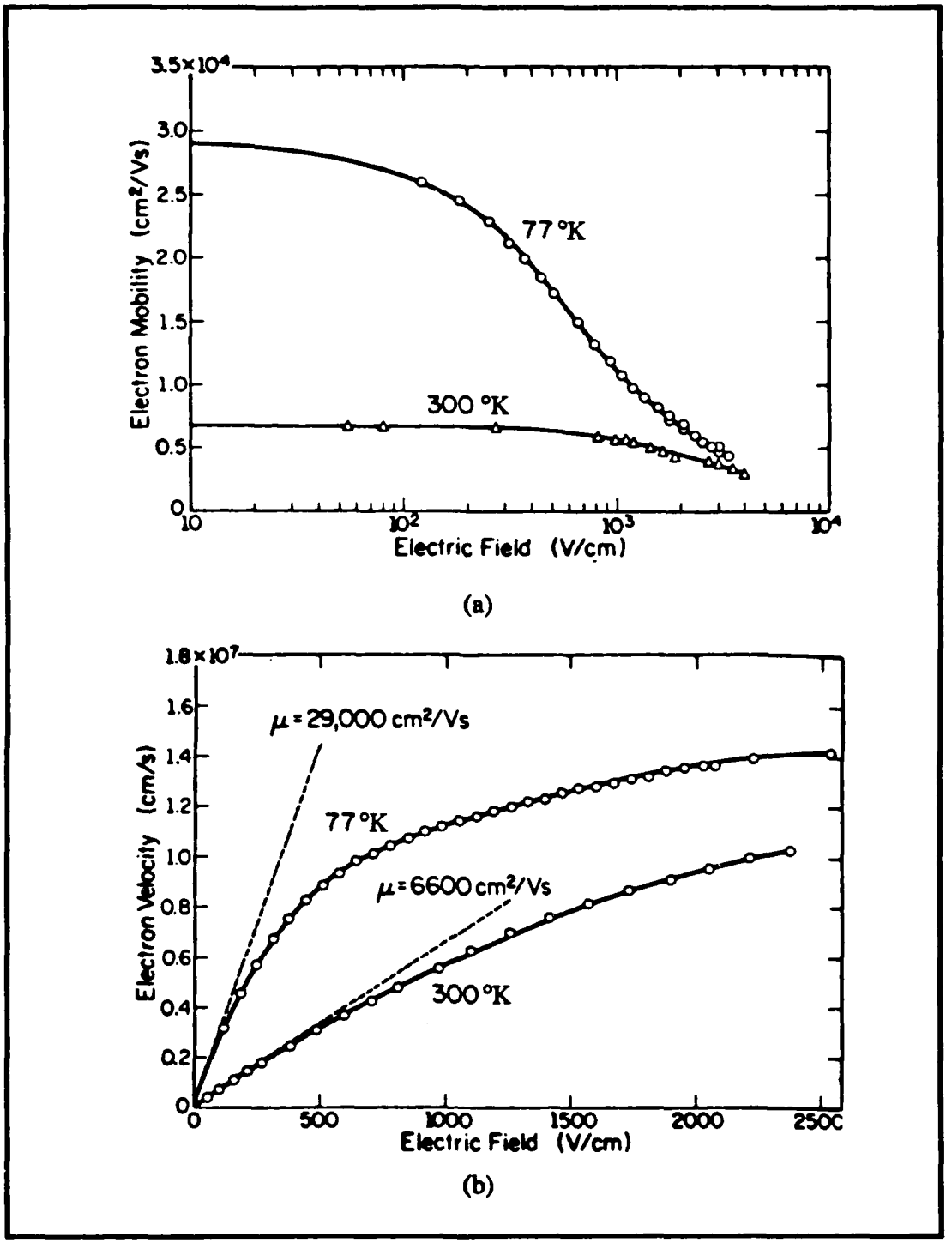

Fig. 2.19 (a) Electron Mobility and (b) Electron Velocity vs. Electric Field at 77 and 300 °K for an InGaAs/AlGaAs Pseudomorphic MODFET Structure [46:565]

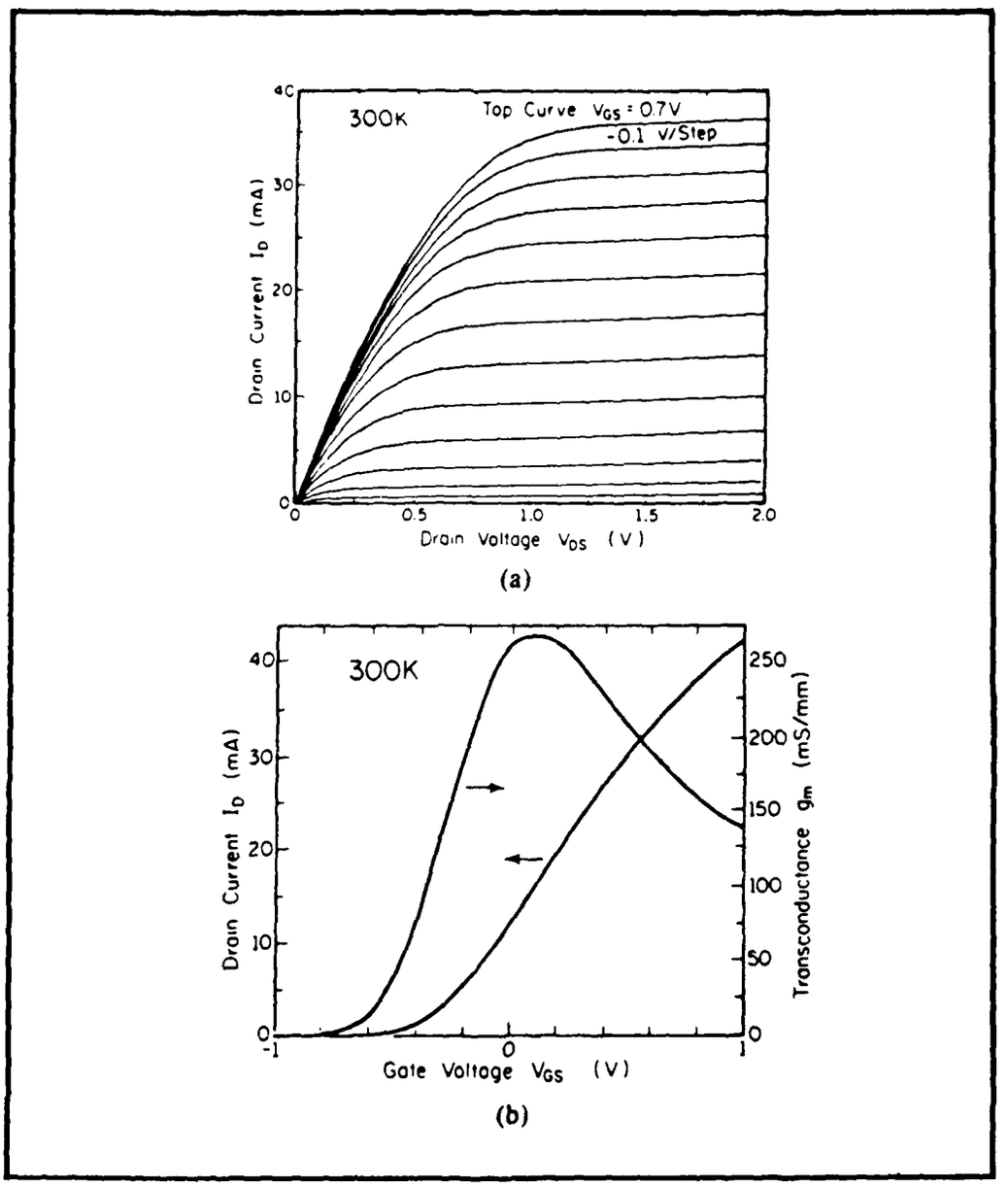

Fig. 2.20 (a) I-V Characteristics and (b) Transfer Characteristics for a 1 x 145 μm^2 InGaAs/AlGaAs Pseudomorphic MODFET. The Source-Drain Spacing was 3 μm and the Peak Transconductance was 270 mS/mm at V_{DS} = 2 volts [46:567]

voltage of 0.1 volts and a drain current density of 100 mA/mm^2 for an InAs mole fraction of y = 0.15. Table 2.1 summarizes the measured effect of InAs mole fraction on transconductance (g_m) at 300 and 77 °K. The g_m is shown to increase as y increases (except for the y = 0.1 sample due to under etching of the gate recess) [46:567]. The drain I-V characteristics of a 0.25 x 50 μm^2 gate $In_{0.15}Ga_{0.85}As$/ $Al_{0.15}Ga_{0.85}As$ pseudomorphic MODFET may be found in [35:650].

The microwave characterization of pseudomorphic MODFETs proceeds as for the normal MODFET. Typically, the MODFET's S-parameters are measured (1 to 26 GHz) and the current gain (h_{21}) and maximum available gain (G_{max}) are then calculated. Table 2.2 lists the small-signal equivalent circuit elements for the $In_yGa_{1-y}As/Al_xGa_{1-x}As$ ($0 \leq y \leq 0.2$) structure of Fig. 2.17 as derived by Ketterson et al. [46:569]. The circuit elements correspond to those of the previously described MODFET circuit model of Fig. 2.14. The maximum power gain frequency (f_{max}), found by extrapolating G_{max} to zero at a slope of - 6 dB per octave, was found to be 40 GHz at y = 0.2 (a 30 percent performance gain over normal MODFETs of equivalent gate geometries) [46:569]. Similarly, the maximum forward current gain frequency (f_T) was found to be 24.5 GHz (a 100 percent performance gain over normal MODFETs of equivalent gate geometries). The results indicate that f_{max} and f_T increase as y increases.

Summary of MODFET Performance

The fundamental theory and measured characteristics of normal, enhanced Schottky-barrier (ES), and pseudomorphic MODFETs have been presented. To conclude this chapter, several MODFET parameters and figures of merit, for a variety of experimental and commercial MODFET device structures, were compiled and are presented in Table 2.3.

Table 2.1

Effect of Indium Arsenide Mole Fraction on DC Transconductance [46:567]

y	300 °K		77 °K	
Percent InAs	Scaled g_m (mS/mm)	V_{OFF} (volts)	Scaled g_m (mS/mm)	V_{OFF} (volts)
5	253	- 0.24	303	- 0.13
10	234	- 0.99	276	- 1.03
15	270	- 0.33	360	- 0.19
20	310	- 0.32	380	- 0.27

Table 2.2

Equivalent Circuit Parameters for Pseudomorphic MODFETs

with Increasing Indium-Arsenide Mole Fractions [46:569]

Parameter	Device					Unit
InAs	0	5	10	15	20	Percent
V_D	2.5	2.5	2.5	2.5	2.5	volts
V_G	0.0	0.0	0.0	0.0	0.0	volts
I_D	43.0	37.0	23.0	45.0	24.0	mA
g_{mo}	42.75	80.80	76.72	77.94	81.01	mS
C_{gs}	0.54	0.69	0.67	0.58	0.53	pF
t	3.26	3.87	4.38	4.23	3.90	psec
C_{dg}	29.28	21.19	43.94	32.82	35.84	fF
C_{ds}	50.29	63.87	61.13	62.62	62.76	fF
G_d	2.51	4.00	2.51	2.87	2.82	mS
R_i	1.04	1.20	1.16	1.20	1.20	Ω
R_g	4.82	5.67	5.79	7.05	7.31	Ω
R_d	7.80	7.26	6.66	6.49	6.40	Ω
R_s	1.95	3.09	3.53	3.39	3.39	Ω
L_g	26.57	26.29	27.97	22.88	22.82	pH
L_d	48.47	49.49	40.28	35.16	34.90	pH
L_s	10.05	13.58	10.45	10.36	10.45	pH
f_{max}	30.5	36.0	34.5	37.0	40.0	GHz
f_T	12.0	19.0	18.5	21.5	24.5	GHz

Table 2.3

Compilation of MODFET Parameters and Figures of Merit.

All Measurements Taken at 300 °K (Measurements at 77 °K Denoted by an †)

Device [Reference]	Scaled g_m (mS/mm)	f_{max} (GHz)	μ_n (cm^2/V-s)	n_s (cm^{-2})	NF (dB)	Gate Length x Width (μm^2)
$Al_{0.3}Ga_{0.7}As$/ GaAs [4]	140	38	-	-	-	1 x 290
$Al_xGa_{1-x}As$/ GaAs [38]	230	-	-	-	0.95 (12 GHz)	0.5 x 200
$Al_{0.28}Ga_{0.72}As$/ GaAs [87]	≈ 160	≈ 88.5	60000†	-	1.2 (12 GHz)	0.5 x 280
p-$Al_{0.52}Ga_{0.48}As$/ GaAs [39]	38	-	170 (μ_p)	5.3 x 10^{11}	-	1 x 50
Al GaAs/GaAs (Multi-Channel) [79]	320 (Two-Channel)	-	5000	5.3 x 10^{12} (Six-Channel)	-	1 x 50
$Si_{1-x}Ge_x$/Ge [18]	36	-	-	-	-	1.5 x 160
$Al_{0.3}Ga_{0.7}As$/GaAs (ESMODFET)[70]	≈ 125	-	-	-	-	2 x 100
$Al_xGa_{1-x}As$/GaAs (ESMODFET)[67]	310	-	-	-	1.2 (12 GHz)	0.5 x 200
$In_{0.15}Ga_{0.85}As$/ GaAs [73]	≈ 90	-	4000	5 x 10^{11}	-	2 x 50
$In_{0.15}Ga_{0.85}As$/ $Al_{0.15}Ga_{0.85}As$ [46]	270	37	6000	1.4 x 10^{12}	-	1 x 145
$In_{0.15}Ga_{0.85}As$/ $Al_{0.15}Ga_{0.85}As$ [35]	480	≈ 200	4210	4.5 x 10^{12}	0.9 (18 GHz)	0.25 x 150
$In_{0.15}Ga_{0.85}As$/ $Al_{0.15}Ga_{0.85}As$ [88]	-	230	-	-	2.1 (62.2 GHz)	0.25 x 50

III. Strained Channel MODFET Design

This chapter discusses the design of a graded-layer $In_yGa_{1-y}As/Al_xGa_{1-x}As$ enhanced Schottky-barrier pseudomorphic (ESP)MODFET. First-order charge-control equations (Appendices A and B) were developed to model the MODFET's energy band characteristics and to determine device parameters for MBE-growth. These parameters include the epitaxial layer thicknesses, material compositions, and doping densities. This chapter is divided into four main sections. First, a review of some material parameters associated with the $In_yGa_{1-y}As$ and $Al_xGa_{1-x}As$ material systems is presented. Next, several aspects of strained-layer superlattices are discussed. The third section outlines the MODFET charge-control equation derivation. The final section shows how the charge-control equations were applied to determine the MBE-growth parameters for the starting material ("layer"), upon which the MODFETs were fabricated.

Material Design Parameters

A review of the material parameters of the $Al_xGa_{1-x}As$ and $In_yGa_{1-y}As$ systems for device applications may be found in [1] and [2], respectively. The material parameters of interest to the MODFET designer include: the bandgap energy, the lattice constant, and the permittivity.

Bandgap Energy. A fundamental parameter of semiconductors is the energy bandgap. A plot of the energy bandgap (direct bandgap) as a function of lattice constant for several compound (III-V) semiconductors is shown in Fig. 3.1. It is seen that the bandgap of the ternary compound $Al_xGa_{1-x}As$ may be varied between 1.42 eV (GaAs) and 2.2 eV (AlAs) by varying the aluminum/gallium ratio (e.g. AlAs mole fraction). As previously shown, the bandgap energy of $Al_xGa_{1-x}As$ (300 °K) may be approximated by [1:R9]

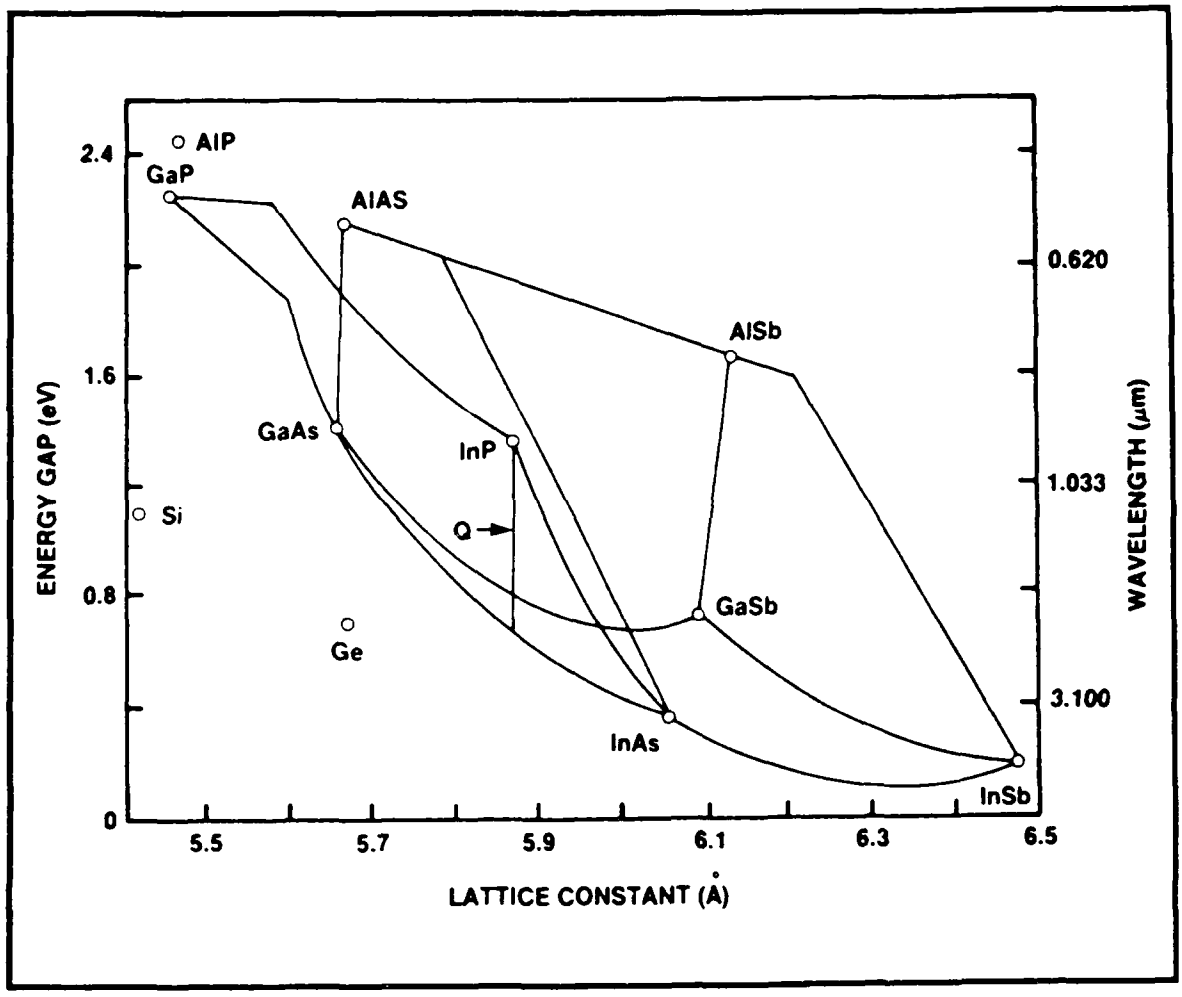

Fig. 3.1 Plot of the Energy Gap vs. Lattice Constant for Several III-V Semiconductors. The Lines that Connect Points on the Graph Show How the Bandgap and the Lattice Constant Vary for Mixtures of the Binary Compounds and for Quaternary Compounds (Q) to which the Points Correspond. Also Shown are the Bandgap and Lattice Constant for the Elemental Semiconductors Silicon and Germanium [66: 98]

$$E_g(x) = 1.424 + 1.247x \quad (eV) \qquad (0 \le x \le 0.45)$$

$$= 1.424 + 1.247x + 1.147(x - 0.45)^2 \quad (eV) \qquad (0.45 \le x \le 1) \tag{2.1}$$

In general, the change in bandgap energy between intermediate ternary compositions of III-V binaries (such as GaAs and AlAs) is nonlinear and maintains a quadratic dependence on the mole fraction. A semiconductor's bandgap determines the energy (or wavelength) at which the material absorbs or emits light [69:14]. The bandgap may be periodically altered (tailored) to yield a new electronic band structure. The electrical and optical properties of ternary or quaternary (Q) compounds may be controlled on the atomic level via a heteroepitaxial growth process, such as MBE. For the present case of interest, an artificially structured n-$Al_xGa_{1-x}As/In_yGa_{1-y}As$/GaAs single quantum potential well material system is desired. The bandgap energy of $In_yGa_{1-y}As$ may be approximated by [2:8780; 86:994]

$$E_g(y) = 1.424 - 1.615y + 0.555y^2 \quad (eV) \qquad (0 \le y \le 1) \tag{3.1}$$

The resultant conduction band discontinuity (ΔE_c) between an $In_yGa_{1-y}As/Al_xGa_{1-x}As$ heterojunction is then [86:994]

$$\Delta E_c = \kappa(1.247x + 1.615y - 0.555y^2) \quad (eV) \qquad (0 \le y \le 1), (0 \le x \le 0.45) \tag{3.2}$$

where κ is in general, a complicated function of x and y that varies with interfacial strain due to the lattice mismatch. By letting $\kappa = 0.7$ and $x = y = 0.15$ in (3.2), it is found that $\Delta E_c = 0.292$ (eV) which is close to the latest value of 0.3 (eV) reported in the literature [46:564]. Alternately, a 65:35 rule may be used such that $\kappa = 0.65$, and thus, the

conduction band discontinuity is 65 percent of the total difference in the bandgaps of the two materials. The conduction band discontinuity ΔE_c (eV) between GaAs and $Al_xGa_{1-x}As$ may be approximated by [1:R11]

$$\begin{aligned} \Delta E_c(x) &= 1.1x \quad (eV) && (0 \le x \le 0.45) \\ &= 0.43 + 0.14x \quad (eV) && (0.45 \le x \le 1.0) \end{aligned} \tag{3.3}$$

Lattice Constant. Strained-layer superlattices (one period in this case) consist of alternating epitaxial layers of two or more materials with different equilibrium lattice constants [69:14]. The lattice constant parameter (a) in many of the III-V compounds is known to obey Vegard's rule, i.e., the lattice parameter varies linearly with composition [1:R5]. The lattice constant of $Al_xGa_{1-x}As$ is then [1:R3]

$$a = 5.6533 + 0.0078x \quad (Å) \quad (0 \le x \le 1) \tag{3.4}$$

Thus, the lattice mismatch of $Al_xGa_{1-x}As$ is less than 0.2 percent throughout the entire compositional range ($0 \le x \le 1$). Using Vegard's rule, the lattice constant of $In_yGa_{1-y}As$ (varying between GaAs (a = 5.6533 Å) and InAs (a = 6.0584 Å) [2:8777]) was computed to be

$$a = 5.6533 + 0.4051y \quad (Å) \quad (0 \le y \le 1) \tag{3.5}$$

Permittivity. The final material parameter of interest is the permittivity (ε) or dielectric constant. The permittivities of $Al_xGa_{1-x}As$ and $In_yGa_{1-y}As$ also obey Vegard's rule [1:R1]. The static permittivity of $Al_xGa_{1-x}As$ is given by [1:R18]

$$\varepsilon = (13.18 - 3.12x)\varepsilon_o \quad \text{(F/cm)} \tag{3.6}$$

where ε_o is the permittivity of vacuum ($\varepsilon_o = 8.85418 \times 10^{-14}$ F/cm). From Vegard's rule, the static permittivity of $In_yGa_{1-y}As$ varies from that of GaAs ($\varepsilon = 13.18\varepsilon_o$) to that of InAs ($\varepsilon = 14.6\varepsilon_o$) and was computed to be

$$\varepsilon = (13.18 + 1.42y)\varepsilon_o \quad \text{(F/cm)} \tag{3.7}$$

Strained-Layer Superlattices

The purpose of this section is to provide a quantitative verification of the pseudomorphic approximation [42] for a single-period GaAs/InGaAs/AlGaAs strained-layer superlattice. The propagation of strain generated within the InGaAs channel layer has been the subject of controversy in previous studies on pseudomorphic MODFETs [60]. When an epitaxial layer of $In_yGa_{1-y}As$ is grown upon a GaAs substrate, a misfit strain is generated. The strain energy is proportional to the thickness of the epitaxial layer [69:14]. The epitaxial layer is typically much thinner than the substrate, and the strain can be accommodated elastically, plastically, or by a combination of the two [49:5428]. As described in Chapter II (see Fig 2.18), if the epitaxial layer is grown sufficiently thin, uniform elastic strain in the epitaxial layer accommodates the mismatch. The situation for an $Al_xGa_{1-x}As/In_yGa_{1-y}As/GaAs$ heterostructure (3-plate model) is shown in Fig. 3.2. In Fig. 3.2a, an $In_yGa_{1-y}As$ epitaxial layer that exceeds the critical layer thickness has been grown upon a GaAs (assumed infinite) substrate, followed by a thin (about 500 Å or less) $Al_xGa_{1-x}As$ epitaxial layer. If each of the epitaxial layers retains its equilibrium crystalline structure, then rows of misfit dislocations (atoms with only 3 bonding neighbors) will appear approximately every 96th and 93rd row of atoms at the $Al_xGa_{1-x}As/In_yGa_{1-y}As$ and

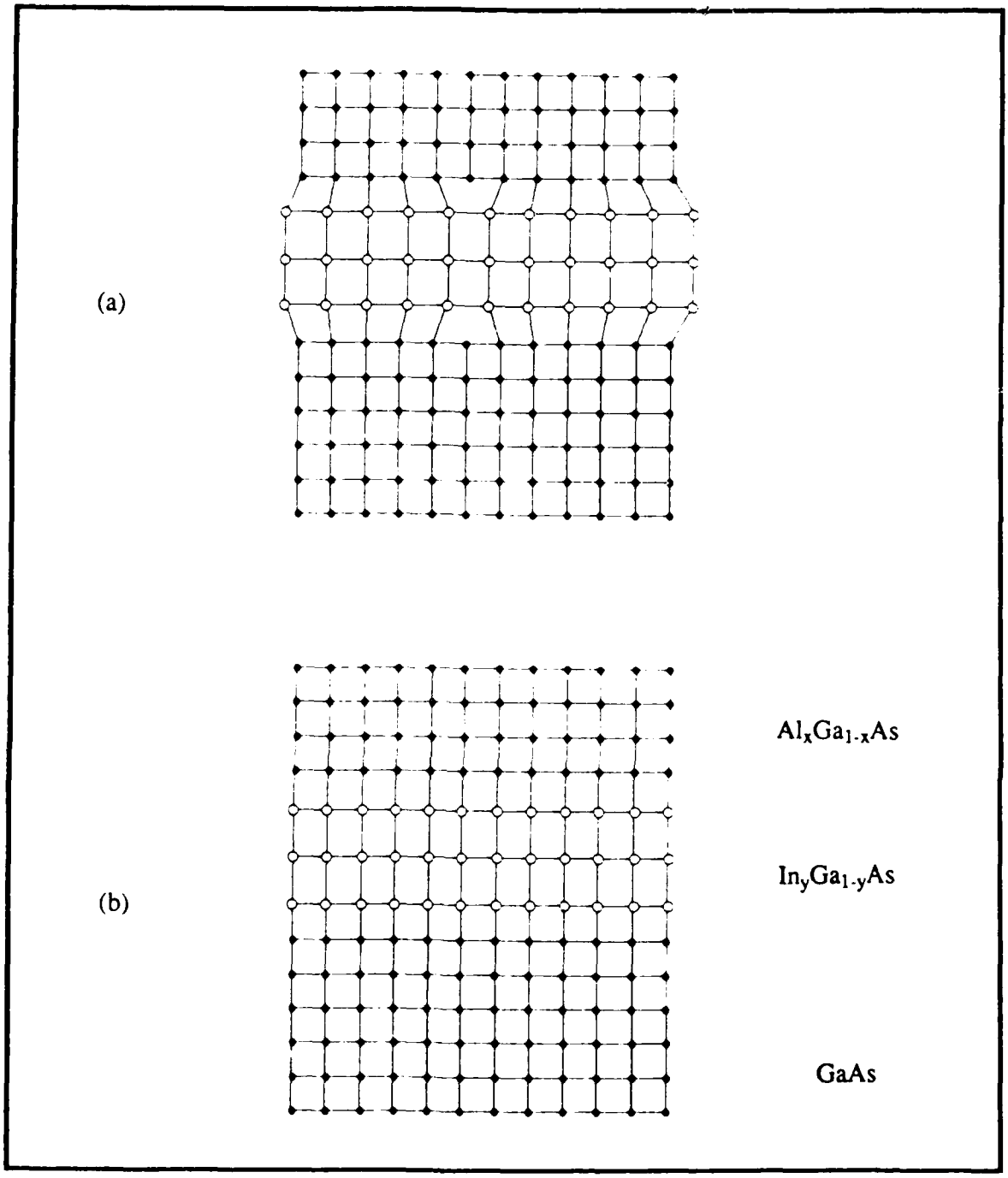

Fig. 3.2 Three-Plate Model of an $Al_xGa_{1-x}As/In_yGa_{1-y}As/GaAs$ Heterostructure. In a), the Misfit Strain Between Epitaxial Layers and the Substrate is Acommodated by Plastic Deformation. In b), the Misfit Strain Between Epitaxial Layers and the Substrate is Acommodated Elastically

$In_yGa_{1-y}As$/GaAs heterointerfaces (assuming x = y = 0.15), respectively. This corresponds to linear misfit dislocation densities of approximately 1.8×10^5 cm^{-1} and 1.9×10^5 cm^{-1}, respectively. The misfit dislocations can degrade the electronic properties of the interface [66:108]. In Fig. 3.2b, an $In_yGa_{1-y}As$ epitaxial layer was grown below the critical layer thickness. The strain in the epitaxial layer is assumed to be entirely elastic (commensurate epitaxy). The four-fold bonding at the hetero-interface will be preserved by compression of the larger $In_yGa_{1-y}As$ lattice along the interfacial plane and by elongation (e.g. tetragonal distortion), due to the Poisson effect, of the $In_yGa_{1-y}As$ lattice planes normal to the substrate [49:5429]. Since the lattice constant of $Al_xGa_{1-x}As$ nearly matches that of GaAs, the final $Al_xGa_{1-x}As$ epitaxial layer is assumed to have been grown coherently (e.g. no dislocations) on the strained $In_yGa_{1-y}As$ epitaxial layer. This is called the pseudomorphic approximation [42].

The growth of unstrained $Al_xGa_{1-x}As$ onto completely elastically strained $In_yGa_{1-y}As$ is justified as follows. Let a_0, a_1, and a_2 equal the equilibrium lattice constants of GaAs, $In_yGa_{1-y}As$ and $Al_xGa_{1-x}As$, respectively. Consider the case of bonding a thin plate (epitaxial layer) of isotropic single crystal (e.g. $In_yGa_{1-y}As$) of size $N_1a_1 \times N_1a_1 \times t_1$ onto a substrate (e.g. GaAs) of different size $N_0a_0 \times N_0a_0 \times t_0$, where N_i is the number of lattice atoms along the edge of the crystal plate, a_i is the lattice constant, and t_i is the thickness of the plate (i = 0 and 1) [16]. The situation is shown in Fig. 3.3, where $a_1 > a_0$. To achieve a coherent interface, N_1 is set equal to N_0. Plates 0 and 1 are bonded together to form a composite plate as follows: equal and opposite forces are applied to the plates to compress Plate 1 and stretch Plate 0 uniformly in the x-y direction to the same final dimension. The two plates are then bonded together with perfect alignment of the atomic planes (Fig. 3.3b). When the applied forces are removed, the moments from the internal elastic stresses bend the composite in the direction shown in Fig. 3.3c. The bending of the composite relaxes

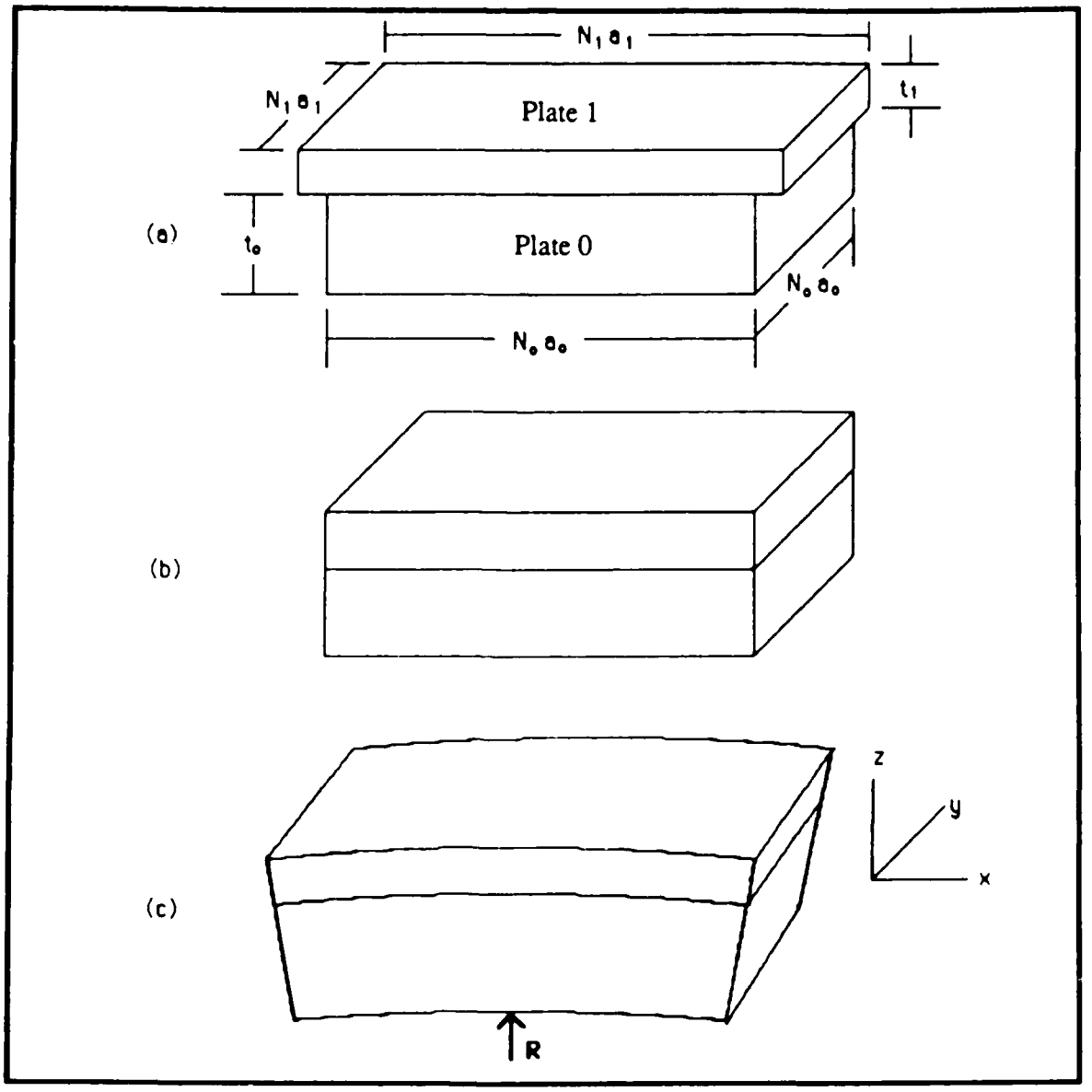

Fig. 3.3 Formation of a Two-Layer Composite: (a) Two Single Crystal Plates with Lattice Constants a_1 and a_0, Number of Atoms Along the Edge N_0 and N_1, and Thickness t_0 and t_1, Respectively; (b) Plate 0 is Stretched and Plate 1 is Compressed to Form an Atomically Matched Composite; (c) the Composite Bends Toward the Side with Smaller Lattice Constant after Removal of the External Stress [16:250]

some of the stress. The composite may be characterized by its radius of curvature (R), which has the following relationship [16:252]:

$$\frac{1}{R} = \frac{6t_1}{t_o^2} \frac{1}{1 + 6\left(\frac{t_1}{t_o}\right)} \cdot \frac{1-\upsilon}{1+\upsilon}\left[\frac{\Delta a_\perp}{a_o} - \rho b_I\right] \quad (m^{-1}) \qquad (3.8)$$

where

υ = Poisson's ratio (assumed equal for all layers) (unitless)

$\Delta a_\perp$ = mismatch of lattice constants perpendicular to the substrate

= $(a_{1\perp epi} - a_{0\perp sub})$ (Å)

ρ = linear density of misfit dislocations (cm^{-1})

b_I = component of the Burger's vector along the hetero-interface (cm)

An expression for $\Delta a_\perp / a_0$ is given by [16:252]

$$\frac{\Delta a_\perp}{a_0} = \frac{1+\upsilon}{1-\upsilon}\frac{\Delta a_r}{a_o} - \frac{2\upsilon}{1-\upsilon}\rho b_I \quad \text{(unitless)} \qquad (3.9)$$

where $\Delta a_r = (a_1 - a_0)$ for $a_1 > a_0$ and $\Delta a_r = (a_0 - a_1)$ for $a_1 < a_0$ is the relaxed lattice mismatch. For the practical case of a 150 Å $In_{0.15}Ga_{0.85}As$ epitaxial layer grown coherently ($\rho = 0$) on a 650 μm GaAs substrate, then from (3.4), (3.5), (3.8), and letting υ = 0.31 [2] and $b_I = a_0$, the radius of curvature is about 436 m. This corresponds to a difference in arclength between the inner and outermost arcs of Fig. 3.3c of less than

0.009 Å. This is far less then the lattice constant of either $In_yGa_{1-y}As$ or GaAs and is verification that the pseudomorphic approximation holds in this case. For this calculation, N_0 and N_1 were set equal to 2.5 cm.

The effect of elastic mismatch strain (ϵ) on the energy bandgap of $In_yGa_{1-y}As$ has been investigated [49]. It was found that the bandgap of a biaxially strained epitaxial layer will be larger than that of an unstrained epitaxial layer when under compression, and smaller when under tension. [49:5428]. This effect has been used to decrease the effective mass of holes in a p-channel MODFET by compressing an undoped $In_yGa_{1-y}As$ quantum well layer between cladding layers of Be-doped GaAs [23]. Biaxial stress splits the valence-band degeneracy by producing anisotropic crystal lattice deformation [49:5428]. A conduction and light-hole valance band recombination process dominates the epitaxial layer under compression (directionally dependent). A conduction heavy-hole valence-band recombination process dominates the epitaxial layer under tension (directionally dependent).

The dependence of energy bandgap shifts of epitaxial layers due to biaxial misfit strain has been investigated by Asai [5]. The bandgap shifts of an epitaxial layer under compression and tension are given by ΔE_{lh} and ΔE_{hh}, respectively. The change in energy between the conduction and valence bands at $\mathbf{k} = 0$ (e.g. direct bandgap), to first order in strain, is given by [5:2055]

$$\Delta E_{lh(compression)} = \left[-2a\left(\frac{C_{11} - C_{12}}{C_{11}}\right) + b\left(\frac{C_{11} + 2C_{12}}{C_{11}}\right)\right]\epsilon \quad \text{(eV)} \qquad (3.10a)$$

$$\Delta E_{hh(tension)} = \left[-2a\left(\frac{C_{11} - C_{12}}{C_{11}}\right) - b\left(\frac{C_{11} + 2C_{12}}{C_{11}}\right)\right]\epsilon \quad \text{(eV)} \qquad (3.10b)$$

where

a = hydrostatic deformation potential

$= -(1/3)(C_{11} + 2C_{12})(\partial E_o/\partial P)$ (eV)

$\partial E_o/\partial P$ = hydrostatic pressure coefficient of the lowest direct energy bandgap (eV/dyn cm^{-2})

C_{ij} = elastic stiffness coefficients (dyn/cm^2)

b = shear deformation potential (eV)

ϵ = misfit strain (unitless)

All the constant terms in (3.10) above are those of the epitaxial layer. Assuming coherent growth, (as in Fig. 3.2b), the strain free lattice constant of the $In_yGa_{1-y}As$ epitaxial layer (a_1) parallel to the hetero-interface is compressed to match the lattice constant of the GaAs substrate (a_0). The misfit strain (ϵ) for a (100) oriented GaAs substrate is then defined as [49:5429]

$$\epsilon = \frac{\Delta a_{sf}}{a_o} = \left[\frac{C_{11}}{C_{11} + 2C_{12}}\right]\frac{\Delta a_{\perp}}{a_o} \qquad \text{(unitless)} \qquad (3.11)$$

where Δa_{sf} is the change in the lattice constant of the strain-free epitaxial layer parallel to the hetero-interface. Thus, ϵ is positive for compressive strain ($a_0 \leq a_1$) and negative for tensile strain ($a_0 \geq a_1$). Note that (3.11) holds only when the misfit strain in the epitaxial layer is accommodated elastically.

For the heterostructure of Fig. 3.2b, the $In_yGa_{1-y}As$ epitaxial layer is under compression and its bandgap is expected to increase. Using the numerical values listed in

Table 3.1, (3.10a), and (3.11), the bandgap increase (ΔE_{lh}) for a compressed $In_yGa_{1-y}As$ epitaxial layer as a function of misfit strain was plotted and is shown in Fig. 3.4 (see Program 1 in Appendix C). The InAs mole fraction (y) was used as a variable parameter. The result is a series of straight lines. For example, when $y = 0.15$, the relation $\Delta E_{lh} = 5.56\epsilon$ (eV) is obtained.

Table 3.1

Material Parameters. List of the Elastic Stiffness Coefficients (C_{ij}), the Hydrostatic Pressure Coefficient of the Lowest Direct Energy Bandgap ($\partial E_o/\partial P$), the Hydrostatic Deformation Potential (a), and the Shear Deformation Potential (b) for AlAs, GaAs, InAs, $Al_xGa_{1-x}As$, and $In_yGa_{1-y}As$. The Values were Obtained from [1; 2] and from Linear Interpolation.

	C_{ij} (10^{11} dyn/cm^2)		$\partial E_o/\partial P$	a	b
Materials	C_{11}	C_{12}	(10^{-12} eV/dyn cm^{-2})	(eV)	(eV)
AlAs	12.02	5.70	10.2	-7.96	-1.5
GaAs	11.88	5.38	11.5	-8.68	-1.7
InAs	8.329	4.526	10.0	-5.79	-1.8
$Al_xGa_{1-x}As$	11.88+0.14x	5.38+0.32x	11.5-1.3x	-8.68+0.72x	-1.7+0.2x
$In_yGa_{1-y}As$	11.88-3.551y	5.38-0.854y	11.5-1.5y	-8.68+2.89y	-1.7-0.1y

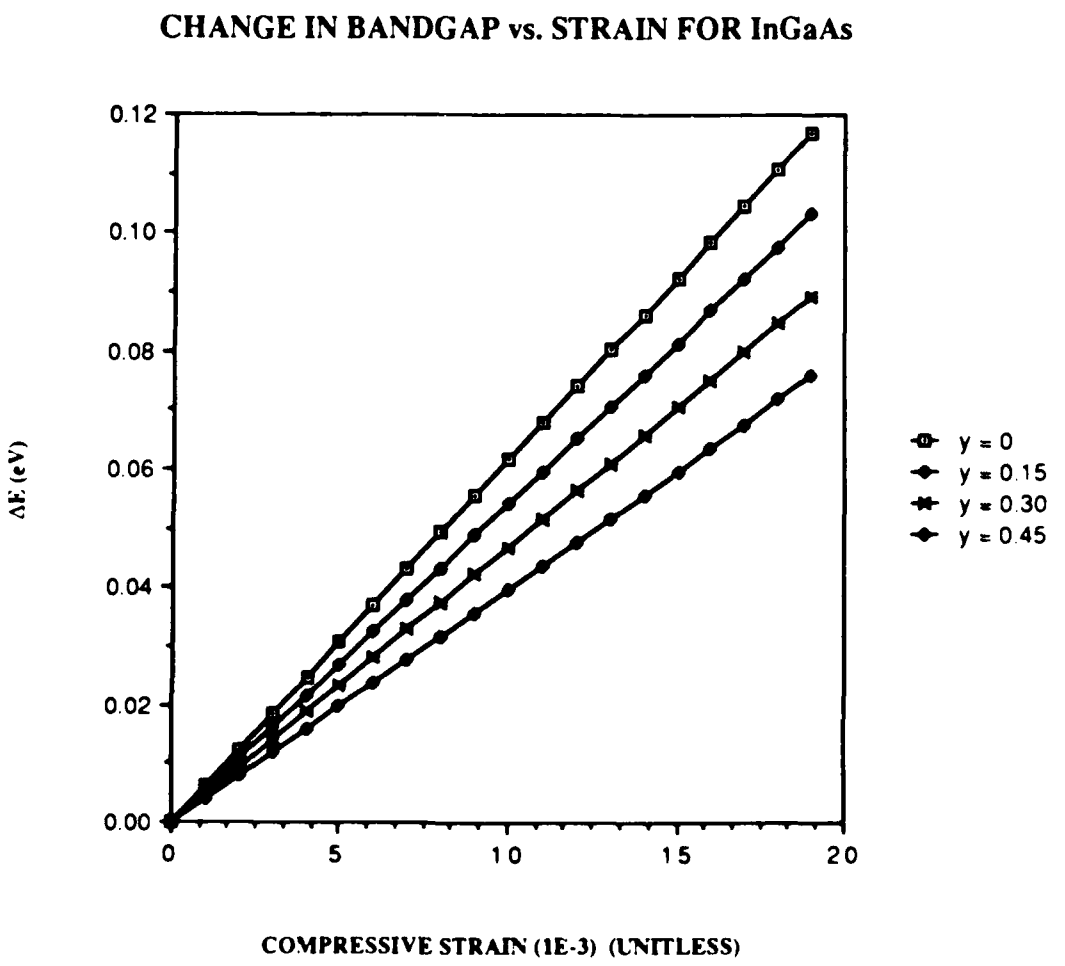

Fig. 3.4 Bandgap Increase of a Compressed $In_yGa_{1-y}As$ Epitaxial Layer Grown Coherently on a Substrate, as a Function of Misfit Strain. The InAs Mole Fraction y is Shown as a Parametric Value

The effect of the strain generated in the "pseudomorphic" InGaAs epitaxial layer upon the subsequent $Al_xGa_{1-x}As$ epitaxial layer(s) is currently under investigation [44]. One may hypothesize a worst case situation where the $Al_{0.15}Ga_{0.85}As$ epitaxial layer has been coherently grown in tension upon the $In_{0.15}Ga_{0.85}As$ epitaxial layer, which has retained its equilibrium lattice constant. Using Table 3.1, (3.10b), and (3.11), one finds that $\Delta E_{hh} = 12.52\epsilon$ (eV) which equals about 0.13 (eV). Thus the energy bandgap of the strained $Al_{0.15}Ga_{0.85}As$ would have been reduced from about 1.61 to 1.48 (eV).

The relationship between the lattice constants parallel to the hetero-interface must be modified when one considers interfacial dislocation densities. For a partially coherent interface (one containing misfit dislocations), an effective lattice constant a* is introduced such that [16:250]

$$a_1^* = a_1 + a_0 \rho b_I \qquad (a_1 < a_0) \qquad (3.12a)$$

$$a_1^* = a_1 - a_0 \rho b_I \qquad (a_1 > a_0) \qquad (3.12b)$$

The mismatch parallel to the interface is then directly related to the dislocation density. When $a_1^* = a_0$, the interface is completely incoherent as in Fig. 3.2a.

A plot of the energy bandgap of strained $In_yGa_{1-y}As$ grown on a GaAs substrate as a function of InAs mole fraction (y) is shown in Fig. 3.5 (the values were calculated using Program 2 in Appendix C). The top curve represents the case of totally elastic strain. The bottom curve represents the case of a totally plastically strained hetero-interface (where $a_1^* = a_0$ and the bandgap of the $In_yGa_{1-y}As$ epitaxial layer is simply equal to its equilibrium value). For the case of a commensurate $Al_{0.15}Ga_{0.85}As$/ $In_{0.15}Ga_{0.85}As$/GaAs heterostructure (as in Fig. 3.2b), the bandgap (totally elastically strained) of

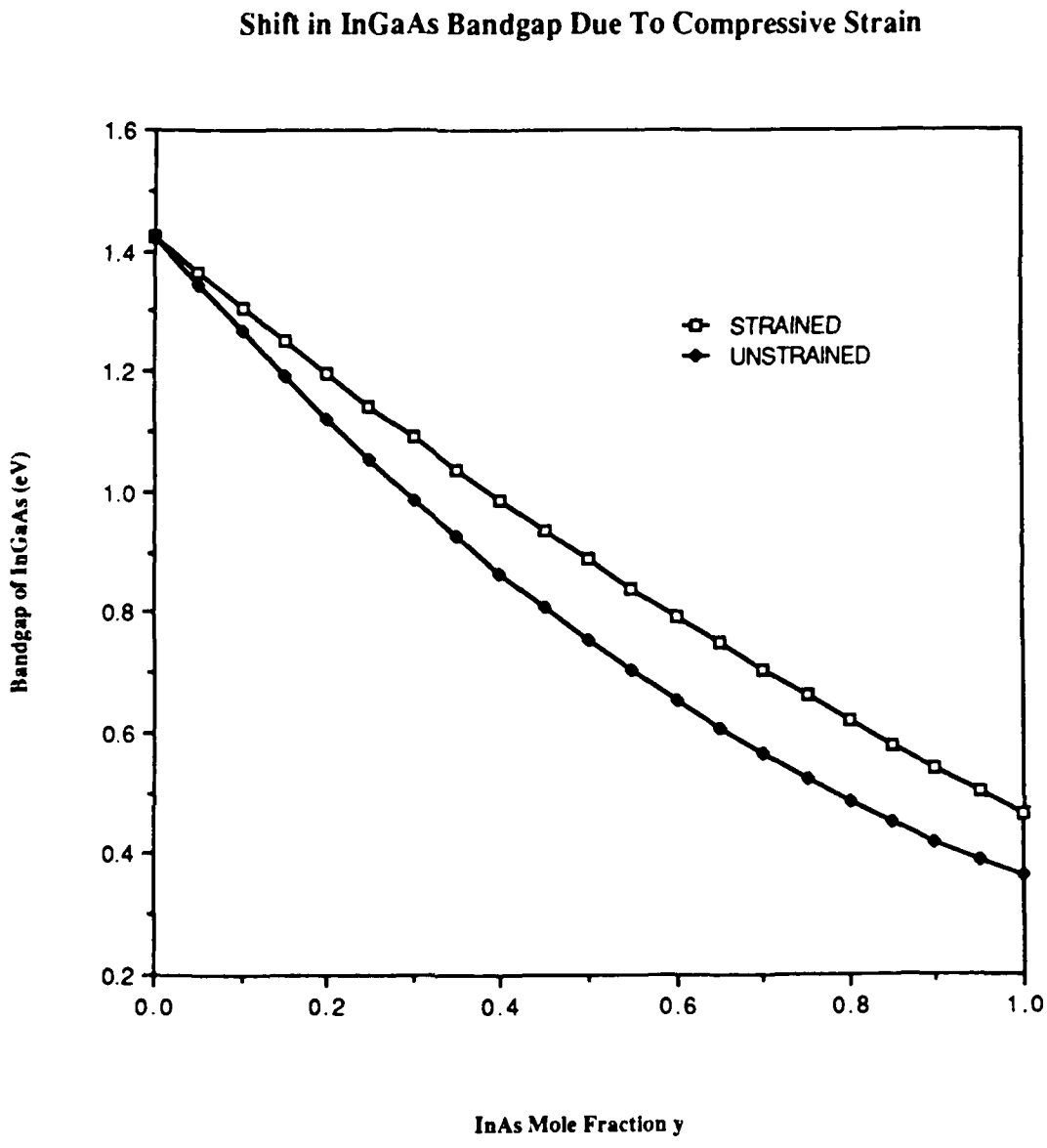

Fig. 3.5 Positive Shift in the Bandgap of a Compressed $In_yGa_{1-y}As$ Epitaxial Layer Grown on a GaAs Substrate. Upper Curve: Total Elastic Strain (Coherent Growth); Lower Curve: Complete Plastic Deformation (Unstrained)

$In_{0.15}Ga_{0.85}As$ is equal to about 1.25 eV, which is about 5 percent larger than its equilibrium value of 1.19 eV, calculated from (3.1).

Charge-Control Equations

The structure of the enhanced Schottky-barrier pseudomorphic (ESP)MODFET used for this study is shown in Fig. 3.6. The structure is based upon past laboratory experience at the University of Illinois [46]. A first-order charge-control Model was developed for the structure shown in Fig. 3.6 in order to quantitatively analyze the effect of adding a p^+-GaAs surface epilayer and a graded n-AlGaAs barrier epilayer to the pseudomorphic MODFET structure previously shown in Fig. 2.17. The (ESP)MODFET structure will first be described. Next, the charge-control model derivation will be outlined. In the next section, the charge-control model will be used to examine the effect of varying the p^+-GaAs doping density and n-AlGaAs barrier layer grading limits on the (ESP)MODFETs threshold voltage, 2DEG density, and effective Schottky-barrier height.

The (ESP)MODFET structure begins with an undoped, (100) oriented GaAs substrate. A Cr-doped S.I. GaAs substrate may also be used. A 10 period superlattice consisting of alternating undoped layers of 50 Å GaAs and 20 Å AlAs may be grown upon the Cr-doped substrate (not needed for the undoped S.I. substrate). The primary purpose for the superlattice (SL) is to reduce impurity diffusion into the epitaxial layers from the substrate [25:7927]. Strained superlattices are known to filter out dislocations (e.g. propagate to the edges) from the substrate [71:24], resulting in a high quality crystalline structure for the subsequent epitaxial layers. Next a 1 μm GaAs buffer layer is grown, followed by a 150 - 200 Å $In_{0.15}Ga_{0.85}As$ quantum well layer. Then, a 30 Å $Al_xGa_{1-x}As$ undoped separation layer is grown, followed by a layer of Si-doped $Al_xGa_{1-x}As$ (200-450 Å). The $Al_xGa_{1-x}As$ layer has been divided into two regions (II and III), the second of which is compositionally graded (a linear grading is assumed). Finally, a Be-doped GaAs cap layer

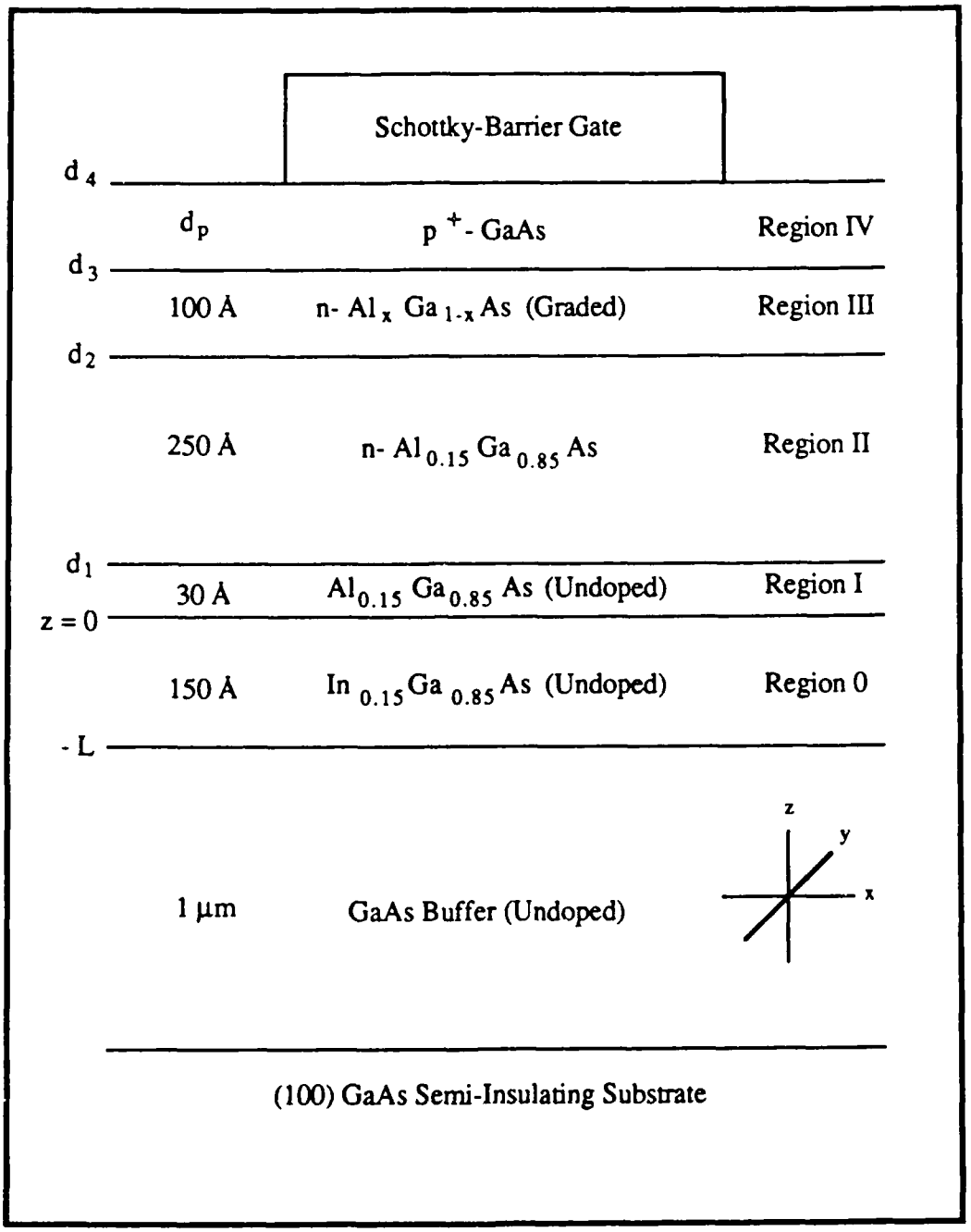

Fig. 3.6 (ESP)MODFET Structure Used in this Study

is grown (50 - 200 Å). Each region is characterized by a permittivity ϵ (F/cm), doping density N_D or N_A (cm^{-3}) (if doped), and thickness d_i (i= 1, 2, 3, or 4) (Å).

The first goal is to obtain a solution (model) to the one-dimensional problem of charge-control by a Schottky-barrier gate. In other words, to find a functional dependence of the 2DEG areal density n_S (cm^{-2}) on the applied gate voltage V_G. The permittivities, doping densities, epitaxial layer thicknesses, Schottky-barrier height, grading function, and structure of the quantum well all serve as variables that affect the dependence of n_s on V_G. The second goal is to model the MODFET's energy band dependence using the above parameters. This will allow one to quantitatively (to first-order) alter the effective Schottky-barrier height of the MODFET via a p^+-GaAs surface layer and a linear grading scheme for part of the n-$Al_xGa_{1-x}As$ barrier layer.

The charge-control model derivation is detailed in Appendices A and B. It begins by solving Poisson's equation for the electric field (E) and electrostatic potential (V) in each region, combined with appropriate boundary conditions. Several assumptions simplify the mathematical charge-control derivation and are outlined in Appendices A and B. Also in Appendix A, the permittivity in Region III is taken as an effective value ϵ_3* (Model 1). In Appendix B, the permittivity in Region III is taken as a function of position $\epsilon_3(z)$ (Model 2). In both cases, the doping distributions are assumed constant throughout a given region and the $In_yGa_{1-y}As$ quantum well layer is assumed to be totally elastically strained (free of misfit dislocations). The $Al_xGa_{1-x}As$ epitaxial layers (and GaAs cap) are assumed to have been coherently grown upon the strained quantum well layer. Initially, energy bandgap shifts due to strained epitaxial layers will be restricted to the $In_yGa_{1-y}As$ layer, as outlined in the second section of this chapter.

The position of the Fermi level relative to the bottom of the conduction band at the $Al_xGa_{1-x}As/In_yGa_{1-y}As$ hetero-interface (ΔE_{F1}) was modelled by (2.2). A self-consistent solution of Schrödinger's and Poisson's equations to determine ΔE_{F1} and the energy levels

of the sub-bands within the quasi-rectangular quantum-well (as required for an exact solution) was not attempted (this has been done by Jaffe [43]). The 2DEG was taken as a sheet charge (x and y direction) at an effective distance (Δd) from the $Al_xGa_{1-x}As$/ $In_yGa_{1-y}As$ hetero-interface. Using the trial data values in Table 3.2, and (A.8), (A.15), (A.23), and (A,31), the electric field vs. gate distance for the MODFET structure of Fig. 3.6 was plotted (see Program 3 in Appendix C) and is shown in Fig. 3.7a. The graded $Al_xGa_{1-x}As$ epitaxial layer (Region III) AlAs mole fraction was varied from $x_1 = 0.15$ at the Region II/III boundary to x_2 ($0 \leq x_2 \leq 1$) at the Region III/IV boundary. The effective permittivity ε_3^* was simply taken as $\varepsilon_3^* = (\varepsilon_3(x_2) + \varepsilon_3(x_1))/2$. Also in Fig. 3.7a, the electric field vs. gate distance using the data values in Table 3.2, and (A.8), (A.15), (B.35), and (B.43) was plotted (see Program 4 in Appendix C). Using the data value in Table 3.2, and (A.37), (A,44), (A.51) and (A.58), the electrostatic potential vs. gate distance was plotted using Model 1 (see Program 5 in Appendix C) and is shown in Fig. 3.7b. Also shown in Fig. 3.7b is the electrostatic potential vs. gate distance obtained from Table 3.2, and (A.37), (A.44), (B.54), and (B.61) using Model 2 (see Program 6 in Appendix C). It was found that the MODFET structure (Fig. 3.6) is adequately modelled by an effective permittivity. The largest difference in the electrostatic potential predicted by the two models with $d_g = 100$ Å is 0.015 eV which is small. Only when d_g is increased to about 1 μm is the difference in the two models noticeable. The values of n_s shown in Table 3.2 were determined from (A.60) and (B.65) for Models 1 and 2, respectively.

These models also show quantitatively to first-order approximation that increasing N_D will increase n_s. Also, increasing the thickness of the separation layer (d_1) will decrease n_s (all other parameters constant). Finally, increasing either N_A or $d_p = (d_4 - d_3)$ will increase the effective Schottky-barrier height. The models are not perfect, however. First, the use of Maxwell-Boltzmann statistics is imprecise for the degenerately doped $Al_xGa_{1-x}As$. Second,

the simple linear relation (2.2) modelling the dependence of ΔE_{F1} on n_s induces an error on the order of 10 percent.

Table 3.2

MODFET Parameters Used to Exercise the Charge-Control Equations.

(Models 1 and 2 Yield Nearly Identical Results)

Parameter	Inputs to Model 1	Inputs to Model 2	Unit
x_1	0.15	0.15	(unitless)
x_2	0.45	0.45	(unitless)
N_D	2×10^{18}	2×10^{18}	(cm^{-3})
N_A	2×10^{19}	2×10^{19}	(cm^{-3})
d_1	30	30	(Å)
$d_2 - d_1$	200	200	(Å)
$d_3 - d_2$	200	200	(Å)
d_p	100	100	(Å)
$q\phi_B$	0.8	0.8	(eV)
Parameter	**Outputs from Model 1**	**Outputs from Model 2**	**Unit**
n_s	1.21×10^{12}	1.22×10^{12}	(cm^{-2})
V_{OFF}*	- 1.07	- 1.08	(volts)
$q\phi_B$*	1.74	1.74	(eV)

AD-A188 828 CHARACTERIZATION OFEENHANCED SCHOTTKY-BARRIER INGAAS/AL(1-X)AS STRINED CH (U) AIR FORCE INST OF TECH WRIGHT-PATTERSON AFB OH SCHOOL OF ENGI J A LOTT 2/3

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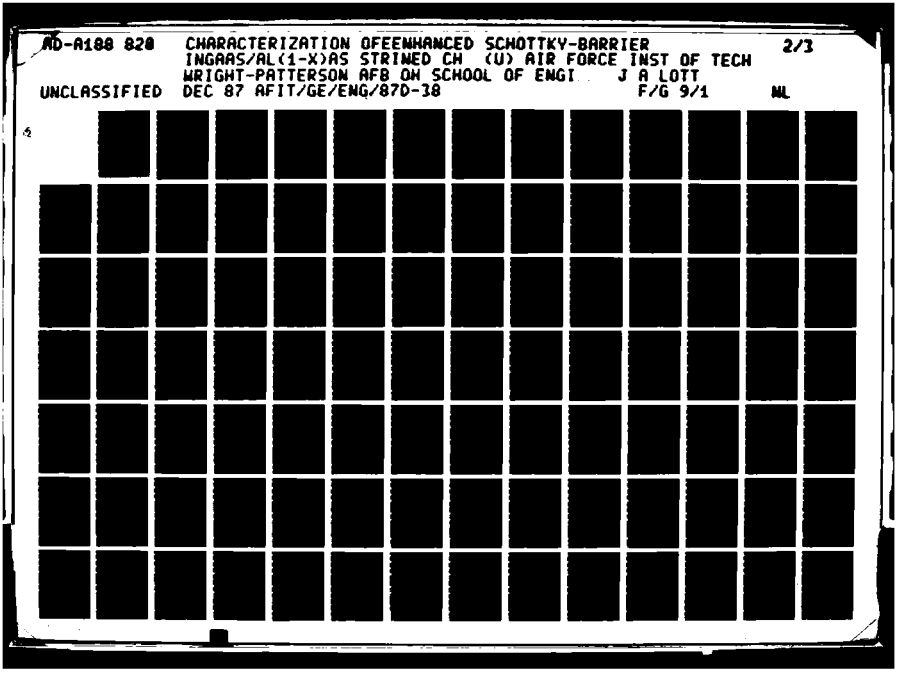

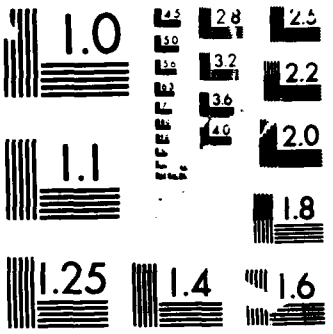

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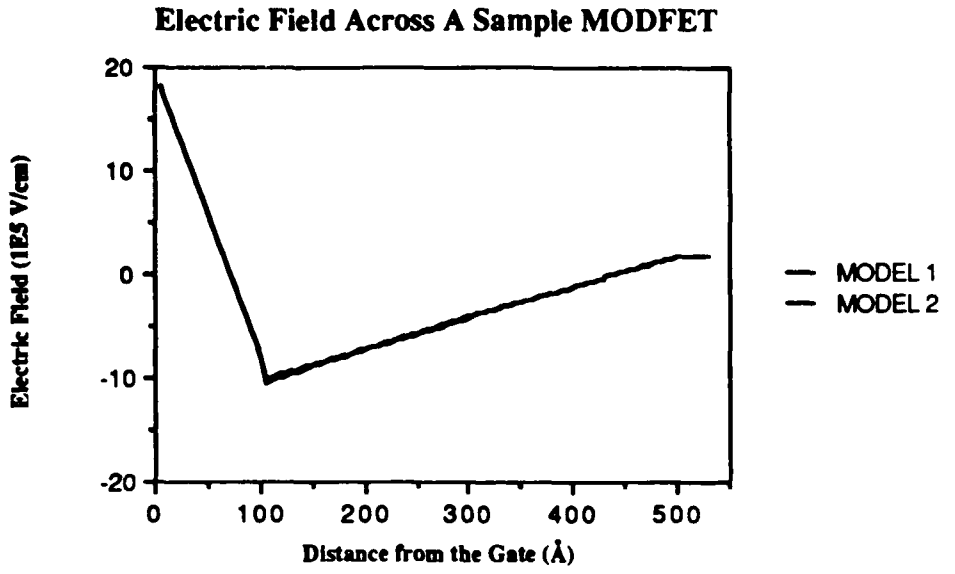
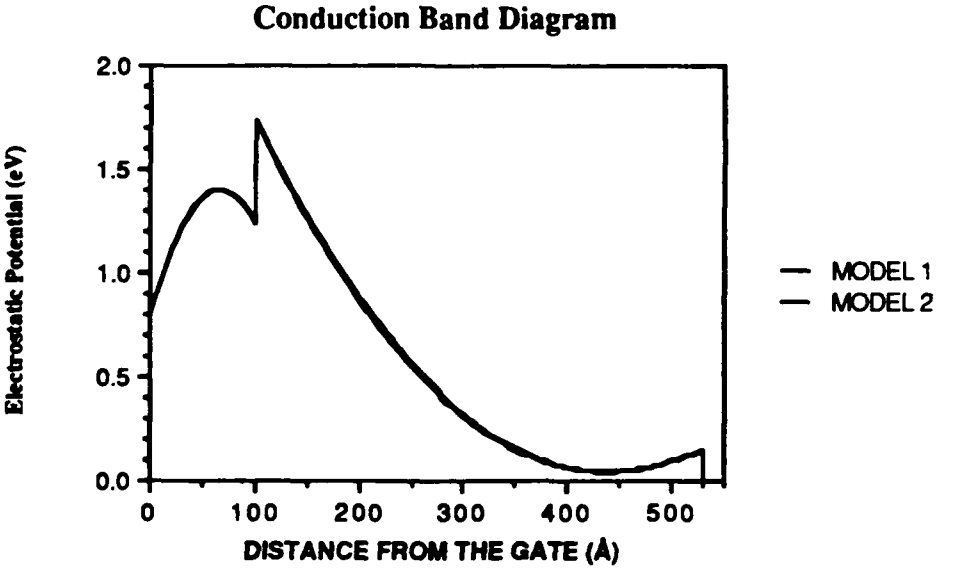


(a)



(b)

Fig. 3.7 Comparison of Charge-Control Models 1 and 2. In (a), Both Models were used to Plot the Electric Field vs. Distance from the Schottky-Barrier Gate using the Values in Table 3.2. In (b), Both Models were used to Plot the Electrostatic Potential vs. Distance from the Schottky-Barrier Gate using the Values in Table 3.2. The Difference in the Two Models is Small

Device Parameters for MBE-Growth

The purpose of this section is to show how Model 2 was used to design the (ESP)MODFET structures used in this study. Model 2 was used to determine the epilayer thicknesses and doping densities, and the grading scheme of the n-AlGaAs barrier epilayer for the structure shown in Fig. 3.6. In order to limit the number of variables in the model and to have a basis (previously fabricated device) for comparison, the variable parameters were limited to N_A, N_D, x_2, and the thickness of Region IV (d_p).

First, Model 2 was used to plot the conduction band diagram of the MODFET structure shown in Fig. 3.6 with $x_2 = 0$, $d_p = 100$ Å, and $N_D = 2 \times 10^{18} cm^{-3}$, as the doping density of the p^+-GaAs epitaxial layer was varied. The result is shown in Fig. 3.8 (it should be noted that Models 1 and 2 fail when the conduction band dips below the Fermi energy level since the models do not account for free electrons). The model predicts that the effective Schottky-barrier height will be a very sensitive function of the parameters N_A and d_p. For example, the value of $q\Delta\phi_B$* when d_p is decreased from 100 Å to 50 Å at $N_A = 2 \times 10^{19} cm^{-3}$, was found to be 1.47 - 0.88 = 0.59 (eV). This is one possible explanation for the reduced effective barrier heights of the (ESP)MODFETs in [60]. As one increases N_A or d_p with all other parameters constant, the effective Schottky-barrier height will increase. Increasing d_p, however, also reduces the MODFET's transconductance. Also, the practical limit of N_A is about $2 - 3 \times 10^{19}$ cm^{-3} [34].

The change in the effective Schottky-barrier height as a function of compositional grading (e.g. as x_2 is varied from 0 to 0.45 while x_1 remains equal to 0.15) of the n-$Al_xGa_{1-x}As$ is shown in Fig. 3.9. It is seen that as the AlAs mole fraction is increased, the barrier for electron transport is also increased, although the change is relatively small. Also, n_s and V_{OFF}* decrease and increase, respectively, as the AlAs mole fraction is increased (all other parameters constant).

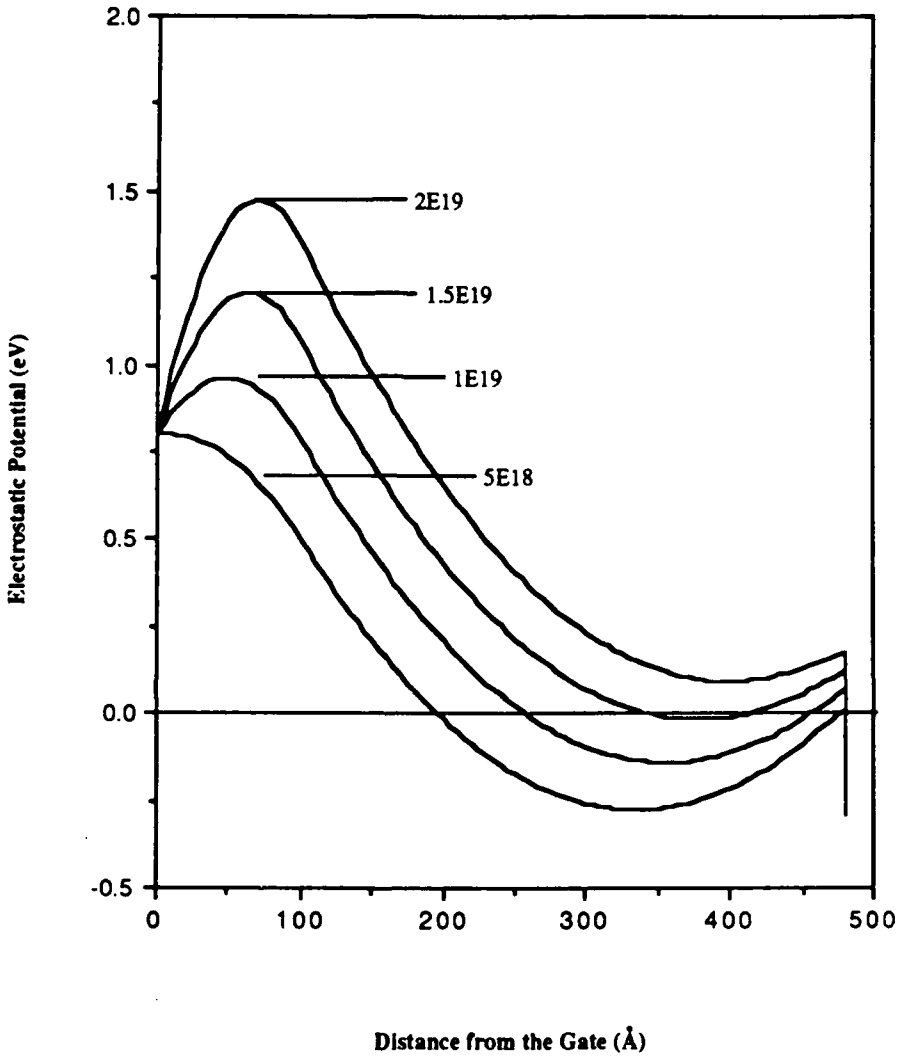


Fig. 3.8 Conduction Band Diagram of an (ESP)MODFET with the p^+-GaAs Doping Density as a Variable. The other Parameters Correspond to Fig. 3.6 with: $x_2 = 0$, $N_D = 2 \times 10^{18}$ cm^{-3}, and $d_p = 100$ Å

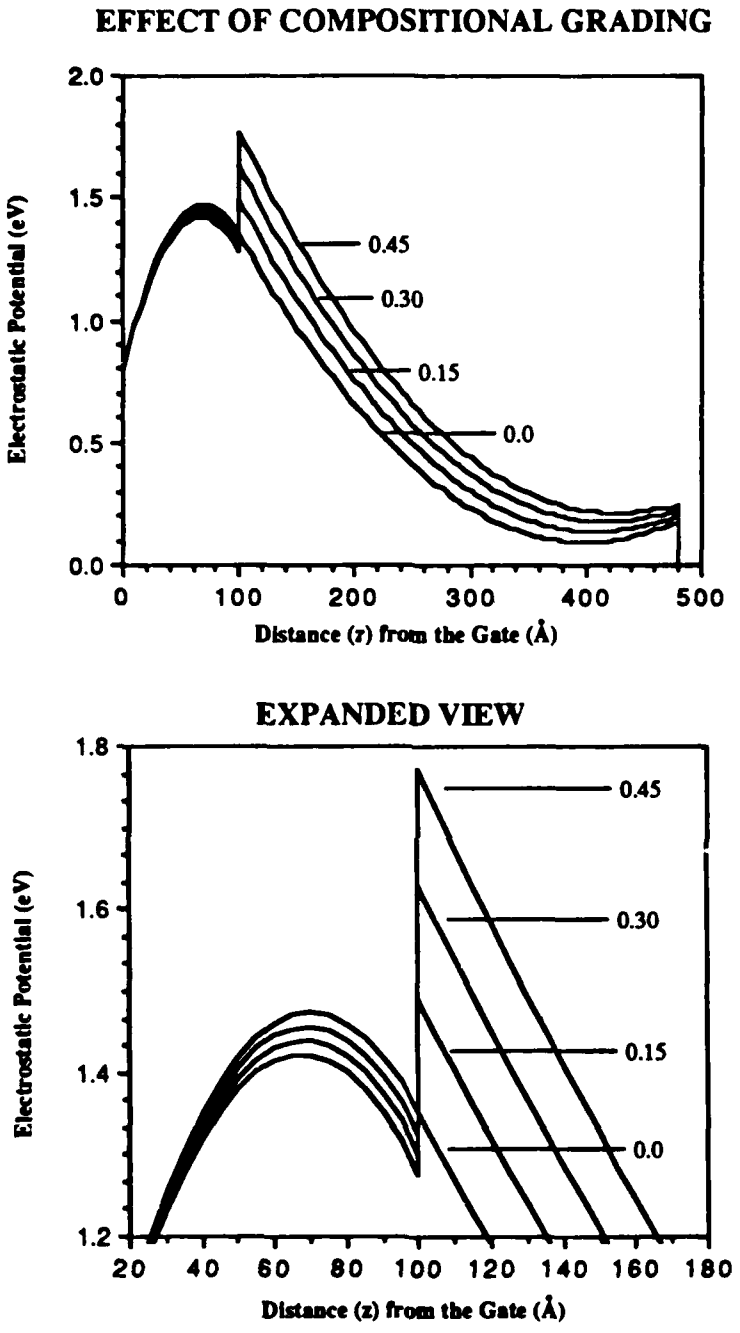


Fig. 3.9 Conduction Band Diagram of an (ESP)MODFET with the Compositional Grading of the $Al_xGa_{1-x}As$ as a Parameter. The other Parameters Correspond to Fig. 3.6 with: $N_D = 2 \times 10^{18}$ cm^{-3} and $d_p = 100$ Å. The Top Curve is $x_2 = 0.45$, Followed by $x_2 = 0.30$, $x_2 = 0.15$, and $x_2 = 0.0$ (Bottom Curve)

Due to the limited number of MBE-growth runs available, a compromise design was chosen in order to fabricate four different depletion-mode MODFET structures from the same basic device structure. The four different structures were used in order to determine the effect of adding a p^+-GaAs epilayer beneath the Schottky-barrier gate of the InGaAs/AlGaAs pseudomorphic MODFET, as well as the effect of linearly grading a portion of the n-AlGaAs barrier epilayer. Model 2 was used to design the four different depletion-mode MODFET structures. The structures included a p^+ (enhanced) -graded test sample and three control samples. The control samples included a graded (unenhanced) control sample (e.g. the same as the test sample only with the p^+-GaAs epilayer removed), a p^+-ungraded control sample (e.g. the same as the test sample with the n-AlGaAs barrier epilayer ungraded), and an ungraded control sample (e.g. the same as the test sample with an ungraded n-AlGaAs barrier layer and with the p^+-GaAs epilayer removed). Depletion-mode devices were chosen to allow for a wider range of gate voltages. The chosen parameters are listed in Table 3.3, along with the expected n_s, V_{OFF}*, and $q\phi_B$* obtained from Model 2. The MBE-grown substrate ("layer") numbers 3379, 3381, and 3408 shown in Table 3.3 are the MBE-growth run designators used by the University of Illinois. As will be described in Chapter IV, the layers were divided into four samples each, and the control samples discussed above were obtained from layers 3379 and 3408 by etching-off the p^+-GaAs epilayer on two of the four samples of each type. Energy band diagrams for the three structures (layers) detailed in Table 3.3 are shown in Fig. 3.10. The conduction bands were first plotted using Model 2, as before, and then the valence bands were added by using (2.1) and (3.1). The design goal was simply to maximize the effective Schottky-barrier height, while keeping the conduction bands of each MODFET type above the Fermi level (since the charge-control model breaks-down at this point).

Table 3.3

MODFET Design Parameters

Parameter	Layer 3379	Layer 3381	Layer 3408	Unit
		INPUTS TO MODEL 2		
x_1	0.15	0.15	0.15	(unitless)
x_2	0.30	0.30	0.15	(unitless)
N_D	2×10^{18}	2×10^{18}	2×10^{18}	(cm^{-3})
N_A	2×10^{19}	NONE	2×10^{19}	(cm^{-3})
d_1	30	30	30	(Å)
$d_2 - d_1$	250	250	250	(Å)
$d_3 - d_2$	100	100	100	(Å)
d_p	100	NONE	100	(Å)
$q\phi_B$	0.8	0.8	0.8	(eV)
		OUTPUTS FROM MODEL 2		
n_s	6.44×10^{11}	1.89×10^{12}	8.3×10^{11}	(cm^{-2})
V_{OFF}*	- 0.52	- 1.25	- 0.67	(volts)
$q\phi_B$*	1.63	0.8	1.49	(eV)

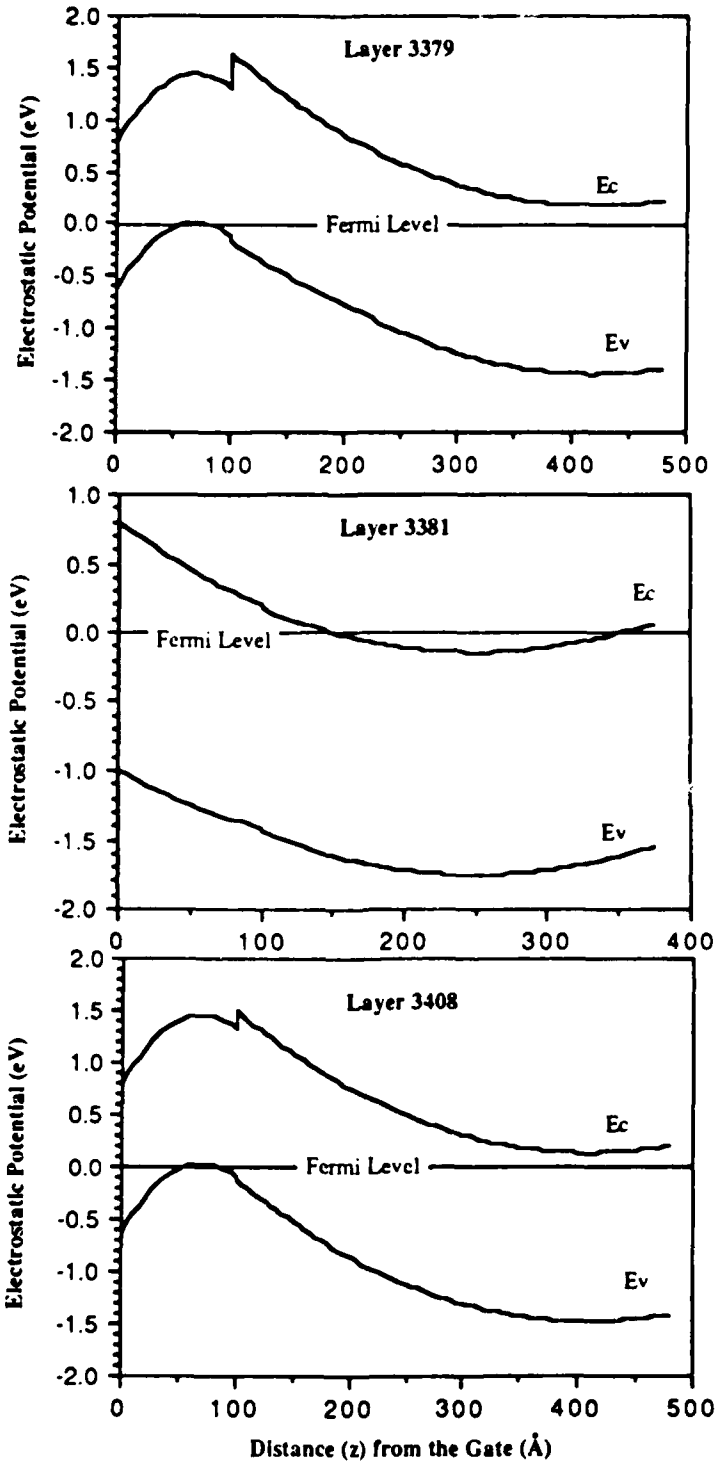


Fig. 3.10 Calculated Energy Band Diagrams for the Three Structures used in this Study (See Table 3.3 for Parameter Values)

IV. Experimental Fabrication and Characterization of the Strained Channel MODFET

This chapter presents the procedures that were used to fabricate and electrically characterize the enhanced Schottky-barrier MODFET structures prepared in this study. The MBE-growth and device fabrication procedures are first described. Next, the methodology and results of both DC and microwave performance measurements are presented. The result is a set of MODFET characteristics (figures of merit) which include: ohmic contact (R_C) and source (R_S) resistance, tranconductance (g_m), unity current gain frequency (f_T), maximum frequency of oscillation (f_{max}), and noise figure (NF).

Fabrication Procedure

The MODFETs were fabricated in two distinct processing sequences. First, the MBE-grown substrates (each called a "layer") were prepared by a crystal-grower [34] at the Cooperative Science Laboratory (CSL), University of Illinois at Urbana-Champaign. Next, MODFETs were fabricated (by the author) on the prepared "layers" at the CSL using established etching, photolithography, and metallization techniques (see Appendix D).

MBE-Growth. Three "layers" were prepared by MBE according to the design specifications listed in Table 3.3 [34]. The MBE system at the University of Illinois is a Riber Model 1000, designed for research activities. Undoped, (100) oriented , GaAs substrates were cleaved into nearly square pieces approximately 2.5 cm on a side. The substrates were then cleaned briefly in a sulfuric acid/hydrogen peroxide/deionized water (DIW) etch (removing about 10 microns from the surface) and placed in hydrochloric acid for one minute to remove surface oxides. Next, the substrates were rinsed in DIW, dried with dry nitrogen gas, and mounted on a molybdenum block with indium solder applied to

the back of the substrate. Finally, the substrates were loaded into the MBE-growth chamber. Growth was achieved by directing thermal beams of semiconductor and impurity elements onto the heated substrate (held at 630 °C). Epitaxial layer growth was controlled by opening and closing effusion cell-shutters. Seven effusion cells were available including: two As cells, a Ga cell, an Al cell, an n-type dopant Si cell, a n-type dopant Sn cell, and a p-type dopant Be cell. The beam fluxes from each effusion cell are exponentially dependent on temperature. The exact dependance varies with the effusion cell elemental source, cell design, the amount of material remaining, and must be determined empirically for each dopant source [23]. The impurity doping levels in the epitaxial layers are determined by the growth rate of the crystal, and the flux density of incident impurity atoms. Growth charts for the "layers" used in this study are shown in Table 4.1. The calibrated cell temperatures are given for each epitaxial layer, along with the epitaxial layer thickness, AlAs mole fraction, and doping level. The arrows in epitaxial layer 5 indicate the ramping of temperature linearly with time in order to produce an approximately linearly graded $Al_xGa_{1-x}As$ region. Not shown is the temperatures of the As effusion cells, which are used for maintaining an arsenic overpressure in the growth chamber. The numbers 3379, 3381, and 3408 in Table 4.1 represent the University of Illinois' MBE-growth run designators.

MODFET Fabrication. After crystal growth, the three prepared "layers" were each divided (cleaved using a diamond tip chisel) into four "samples", about 1 cm^2. The four samples of each "layer" were designated alphabetically (e.g. 3379A, 3379B, 3379C etc.). Individual MODFETs were then fabricated on the 12 samples as outlined below. The details of the MODFET fabrication procedure are given in Appendix D.

The mask set used to fabricate the (ESP)MODFETs is shown in Fig 4.1. The fabrication process for the (ESP)MODFET with a p^+-GaAs surface layer and a graded n-AlGaAs barrier layer (p^+-graded device type) is illustrated in Fig. 4.2. Initially, the indium solder

Table 4.1

MBE-Growth Charts [34]

Cell	Layers 3379 and 3381 (epilayer 6 not included for layer 3381)						
Temp °C	Substrate	1	2	3	4	5	6
Ga	-	925	918	918	918	↓909	909
Al	-	-	-	1040	1040	↑1070	-
Si	-	-	-	-	1128	1128	-
In	-	-	728	-	-	-	-
Be	-	-	-	-	-	-	855
Thickness	-	1 μm	150 Å	30 Å	250 Å	100 Å	100 Å
Mole Fraction	-	-	0.15	0.15	0.15	0.15-0.30	-
Doping Level (cm^{-3})		-	-	-	$2x10^{18}$	$2x10^{18}$	$2x10^{19}$

Cell	Layer 3408					
Temp °C	Substrate	1	2	3	4	5
Ga	-	925	918	918	918	918
Al	-	-	-	1040	1040	-
Si	-	-	-	-	1128	-
In	-	-	728	-	-	-
Be	-	-	-	-	-	867
Thickness	-	1 μm	150 Å	30 Å	350 Å	100 Å
Mole Fraction	-	-	0.15	0.15	0.15	-
Doping Level (cm^{-3})		-	-	-	$2x10^{18}$	$2x10^{19}$

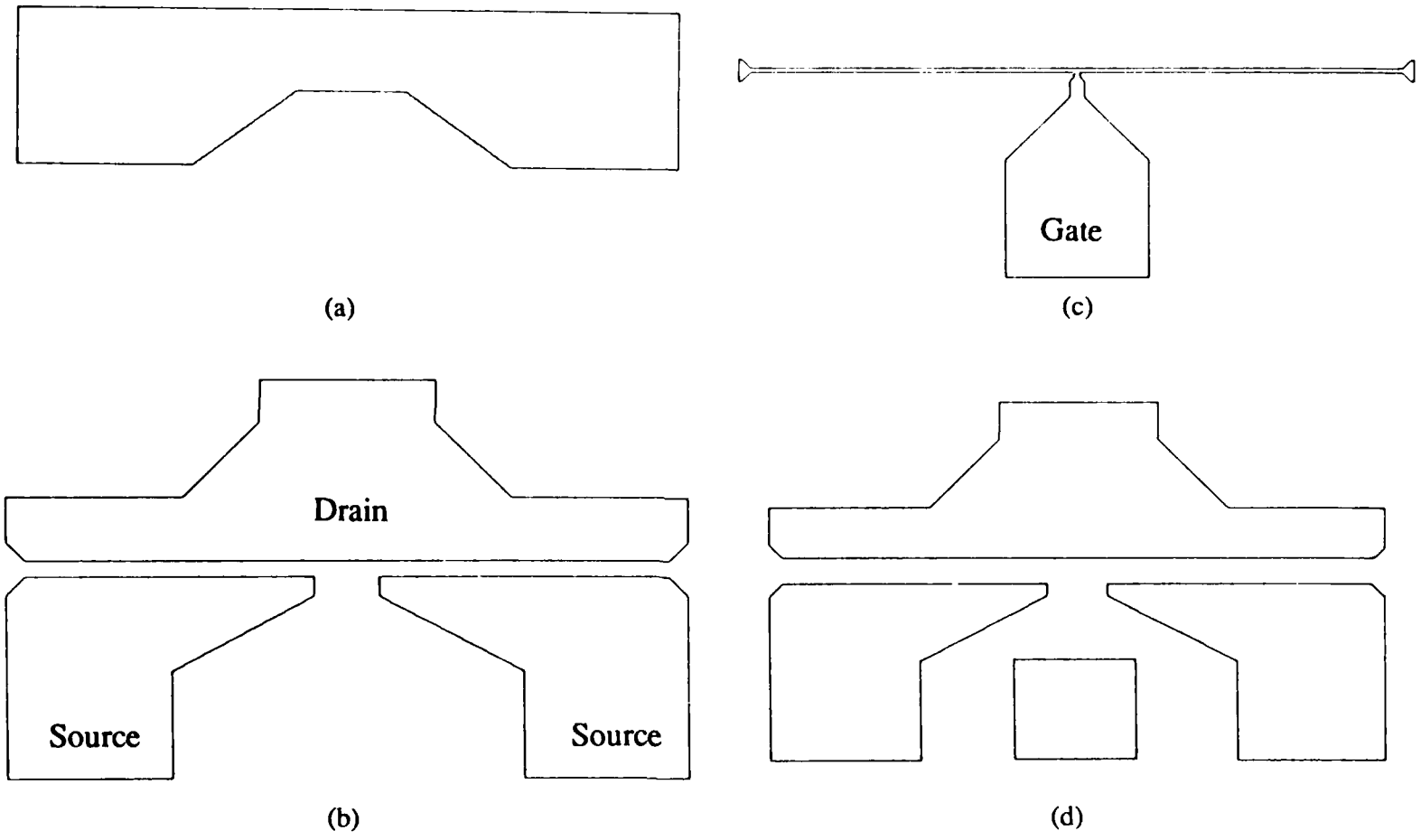


Fig. 4.1 Mask Set Used to Fabricate the MODFETs: (a) Mesa Isolation; (b) Source and Drain Contact; (c) Gate Contact; (d) Overlay Metallization

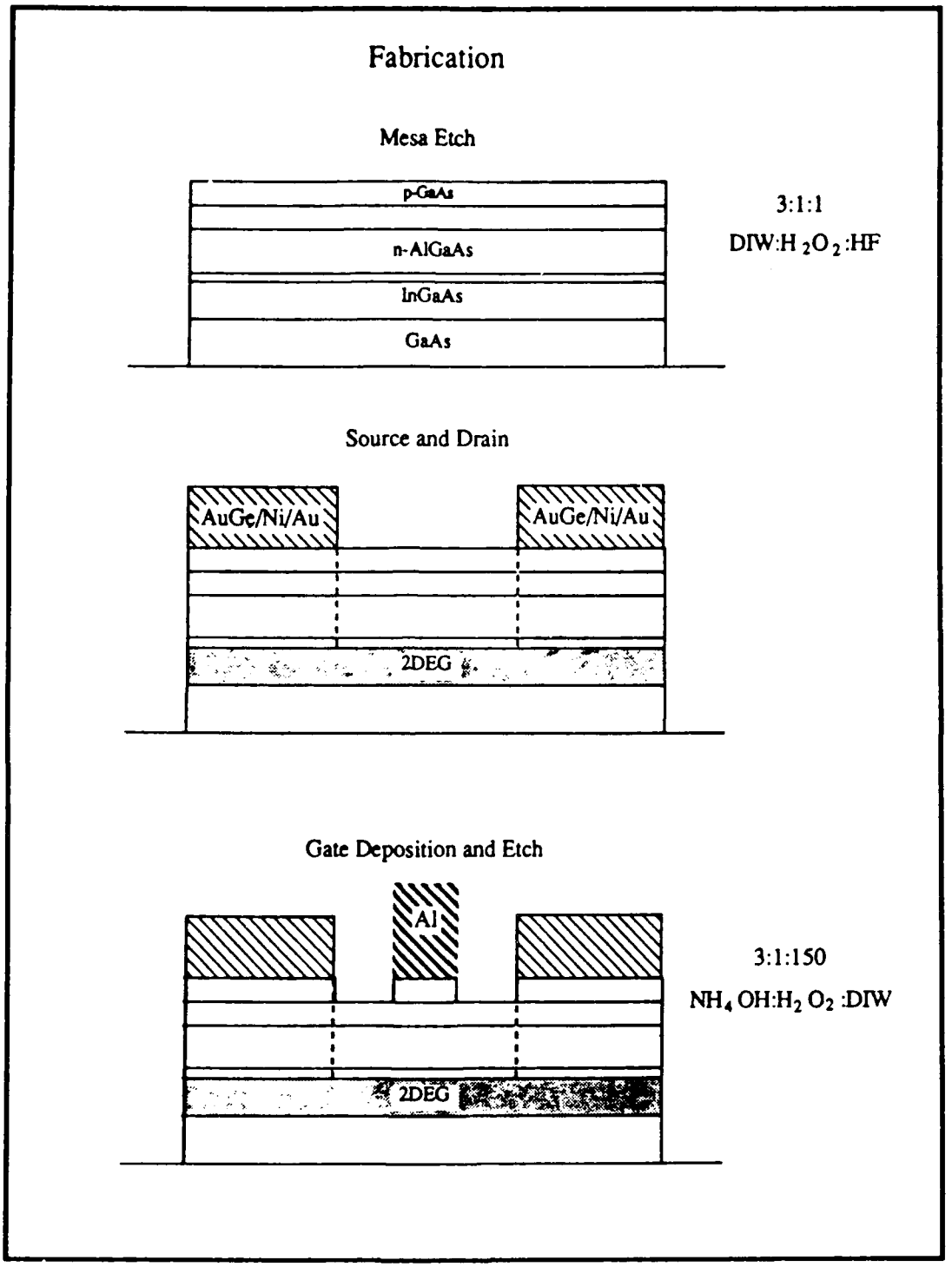


Fig. 4.2 (ESP)MODFET Fabrication Procedure

used to mount the substrate during MBE-growth was removed in a solution prepared by dissolving 1 gram mercuric chloride (H_gCl_2) in 10 ml N,N-dimethyl formamide ($HCON(CH_3)_2$). To facilitate handling, a protective coating of positive photoresist was then placed on the front surface of the samples. The samples were mounted face down onto a metal lapping block using paraffin wax, and then thinned uniformly to about 400 μm (the initial sample thickness was 620-700 μm). The first two steps above provided the samples with smooth back surfaces. This was necessary for accurate photolithographic mask alignment and for establishing a tight vacuum when holding the samples in a photoresist spinner.

The next step involved removal of the entire p^+-GaAs epitaxial layer by etching on samples 3408A and 3408B. These samples were placed in a solution of ammonium hydroxide: hydrogen peroxide: deionized water (NH_4OH:H_2O_2: DIW) in a concentration of 3:1:150 by volume. Based on a GaAs selective etch rate of 30 Å/s, the samples were immersed into the mixture for 3.5 seconds and then immediately immersed in DIW to stop the etch.

The mesa etch was performed on all the samples in order to isolate individual MODFETs. Positive photoresist was spun on the samples and baked. The samples were exposed under the mesa etch mask. The positive photoresist was developed and the exposed areas were etched down into the GaAs buffer epitaxial layer in a beaker of 3:1:1, DIW :H_2O_2: HF (hydrofluoric acid) for 8 seconds. The positive photoresist was removed in acetone, leaving mesas of active material upon which the MODFETs (and test patterns) were fabricated.

Next, source and drain ohmic contacts were patterned onto the samples using positive photoresist and the source/drain metallization mask. The photoresist was developed. The samples were placed in an evaporation chamber and contact metal was evaporated (thermally and by electron-beam) onto the patterned sample surface. The metallization

scheme consisted of the following elements and thicknesses in order: AuGe 400 Å, Ni 100 Å, and Au 600 Å. Next, a positive resist lift-off technique was used, followed by an ohmic contact alloying step. The samples were placed in an alloying oven at 500 °C in a hydrogen atmosphere for 50 seconds. This allowed the Ge in the metal eutectic to diffuse down to the 2DEG in the MODFET's active region, making the source and drain contacts highly n-type. Unfortunately, Ti was accidently substituted for Ni during the metal deposition of two of the samples (3408B and 3408C). For these samples, the source/drain metallization patterns were thin and nonuniform (discolored) after alloying, resulting in poor device performance (as will be shown in the next section on DC testing).

The next step was another p^+-GaAs layer etch for two of the samples, followed by evaporation of Al between the source and drain contacts in order to form Schottky-barrier gates. First, positive photoresist was spun-on the samples. The samples were pre-baked, aligned, and then exposed to the gate mask. After developing the positive photoresist, samples 3379A and 3379B were placed in a beaker of 3:1:150 by volume, NH_4OH:H_2O_2: DIW for 3.5 seconds under ultrasonic agitation. This step selectively removed the p^+-GaAs epitaxial layer (under the gate contact) on the samples. These samples would later serve as control samples for comparison with samples 3379C and 3379D, which both retained p^+-GaAs epitaxial layers underneath the Schottky-barrier gate. Next, the samples were placed in chlorobenzene (C_6H_5Cl) for 15 minutes, re-baked, then placed in the evaporation chamber for evaporation of about 3000 Å of Al. Again, the positive photoresist and patterned gate metal was lifted-off in an ultrasonically agitated acetone soak. The final step (excluding overlay metal evaporation) was the etching of the p^+-GaAs epitaxial layers between the gate and source, and gate and drain on samples 3379C, 3379D, 3408C, and 3408D. These four samples with p^+-GaAs surface epitaxial layers were placed in the 3:1:150 by volume, NH_4OH:H_2O_2:DIW solution under ultrasonic agitation for

3.5 seconds. This step removed the (ESP)MODFET's p-channel parasitic MESFET path. The parasitic MESFET path was also removed from control samples 3379A and 3379B.

The overlay metallization mask was used as before, with positive photoresist, for the select group of samples that would be diced and bonded onto stripline carriers for microwave testing. The overlay metallization mask was used to pattern regions on the gate, drain, and source metallization patterns where thicker metal would be needed to facilitate gold wire bonding. The metallization scheme consisted of a thick Ti/Au overlay (about 500 Å/5000 Å). A summary of the (ESP)MODFET samples fabricated in this work is listed in Table 4.2. When the fabrication was complete, each sample contained about 75 - 100 (ESP)MODFETs with nominal 1 x 290 μm^2 (gate length x width) geometries and 3 μm channels, along with various test patterns and other geometry FETs.

Table 4.2

Summary of (ESP)MODFET Fabrication

Sample	Device Type	Grading	p^+-GaAs Epitaxial Layer Comment
3379A	Graded	0.15 - 0.30	Etched Before Gate Metallization
3379B	Graded	0.15 - 0.30	Etched Before Gate Metallization
3379C	p^+-Graded	0.15 - 0.30	p^+
3379D	p^+-Graded	0.15 - 0.30	p^+
3381A	Graded	0.15 - 0.30	none
3381B	Graded	0.15 - 0.30	none
3381C	Graded	0.15 - 0.30	none
3381D	Graded	0.15 - 0.30	none
3408A	Ungraded	0.15 - 0.15	Etched Before Fabrication
3408B	Ungraded	0.15 - 0.15	Etched Before Fabrication
3408C	p^+-Ungraded	0.15 - 0.15	p^+
3408D	p^+-Ungraded	0.15 - 0.15	p^+

DC Characterization

The fabricated (ESP)MODFETs were characterized by a series of DC measurements. The measurements included the determination of: contact (R_C) and source (R_S) resistance; intrinsic (g_{mo}) and extrinsic (g_m) transconductance; threshold voltage (V_{OFF}); and effective Schottky-barrier height (ϕ_B*). The parameters g_m, V_{OFF}, and ϕ_B* were determined from the following current-voltage (I-V) curves: I_G vs. V_{GS}; I_D vs. V_{GS}; I_D vs. V_{DS}; and from a plot of $g_m = \Delta I_D/\Delta V_{GS}Z$ (mS/mm) vs. V_{GS} where Z is the gate width. Two commercial low-noise microwave transistors, a DXL-0503 MESFET and an MPD-H503 HEMT were also characterized at DC (and later at microwave frequencies). The purpose was to verify the operation of the test equipment by comparing the measured performance with published data. Three devices of each type were used. The DXL-0503 is a GaAs MESFET with a 0.3 μm gate-length and a 280 μm gate-width. The structure and metallization pattern for the MPD-H503 HEMT was shown in Figs 2.1 and 2.3. This HEMT has a gate-length of 0.5 μm and a 280 μm gate-width. Five pieces of test equipment were used for the DC measurements including: an Hewlett-Packard (HP) 4145 semiconductor parameter analyzer; an HP 7475 plotter; a Bausch and Lomb microprobe station; an HP 3465 digital multimeter; and an HP 6181 DC current source. A representative set of I-V curves for several MODFET samples may be found in Appendix E. In the following DC measurement sections, when a mean value is given, it represents the average value of 25 measurements on 25 different devices, all on the same sample. All measurements were performed in the dark at about 300 °K.

I-V Measurements. The samples were placed on the microprobe station. The microprobe station was connected to the HP 4145 via three probes for the source, drain, and gate. Sets of three I-V curves, including a transconductance vs. V_{GS} curve, were taken from each MODFET device as described above. Since the devices had dual source pads,

only half the device was measured which meant that Z = 0.145 mm for the transconductance (scaled) curves. Representative plots of I_G vs. V_{GS} (gate diode), I_D vs. V_{GS} and normalized extrinsic transconductance vs. V_{GS}, and I_D vs. V_{DS} are shown in Figs 4.3 - 4.5, respectively (see also Appendix E).

Effective Schottky-Barrier Height. The effective Schottky-barrier heights ($q\phi_B^*$) were determined from the I_G vs. V_{GS} (V_{DS} = 0) curves (Fig. 4.3). Normal MODFETs have a $q\phi_B^*$ of about 0.8 eV (aluminum gate). The (ESP)MODFETs are expected to have a $q\phi_B^*$ of between 1.4 -1.6 eV. Also, it is expected that the $q\phi_B^*$ of the (ESP)MODFETs with the graded barrier layers (x = 0.15 to 0.30) should be about 0.1 - 0.2 eV higher than those with ungraded barriers. The effective Schottky-barrier height was determined by extrapolating the I_G vs. V_{GS} curve down to the V_{GS} (abscissa) axis. The V_{GS} intersection was taken as ϕ_B^* (volts). The measured effective Schottky-barrier height for each sample is shown in Table 4.3.

Threshold Voltage. The threshold voltages (V_{OFF}) were determined from the g_m vs. V_{GS} plots (Fig. 4.4). A tangent line was drawn to the transconductance curve as it rose above zero. This line was extrapolated down to the V_{GS} axis. The intercept was then recorded as V_{OFF}. Alternately, one could have extrapolated the linear portion of an $(I_D)^{1/2}$ vs. V_{GS} curve near $I_D = 0$ down to the V_{GS} axis. The results are shown in Table 4.3.

Transconductance. The extrinsic transconductance was determined by measuring the change in drain current divided by the change in gate voltage. This value was divided by half the device's gate length (Z = 0.145 mm) to normalize g_m to units of mS/mm. The g_m varies with both V_{GS} and V_{DS}. All plots of g_m were taken with V_{DS} = 1.5 Volts as V_{GS} was swept from about -1.0 to +1.0 Volts. The peak normalized g_m was then recorded, and the results are shown in Table 4.4. Also shown are the calculated intrinsic transconductances, (g_{mo}). The g_{mo}'s were determined from $g_{mo} = g_m/(1 - R_S g_m)$ and the measurements of R_S. The source resistance measurements are described in the next sub-section.

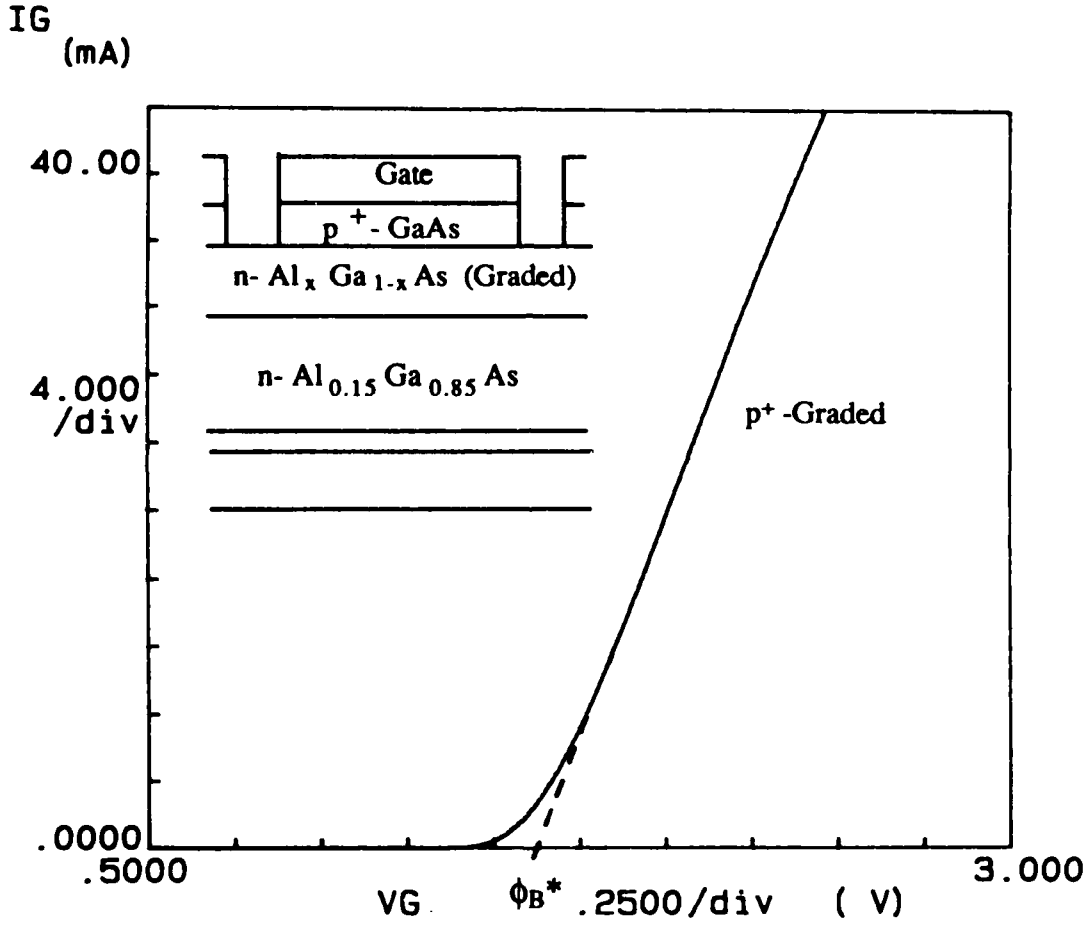


Fig. 4.3 Plot of I_G vs. V_{GS} (with V_{DS} = 0 V) for Sample 3379D (p^+-Graded)

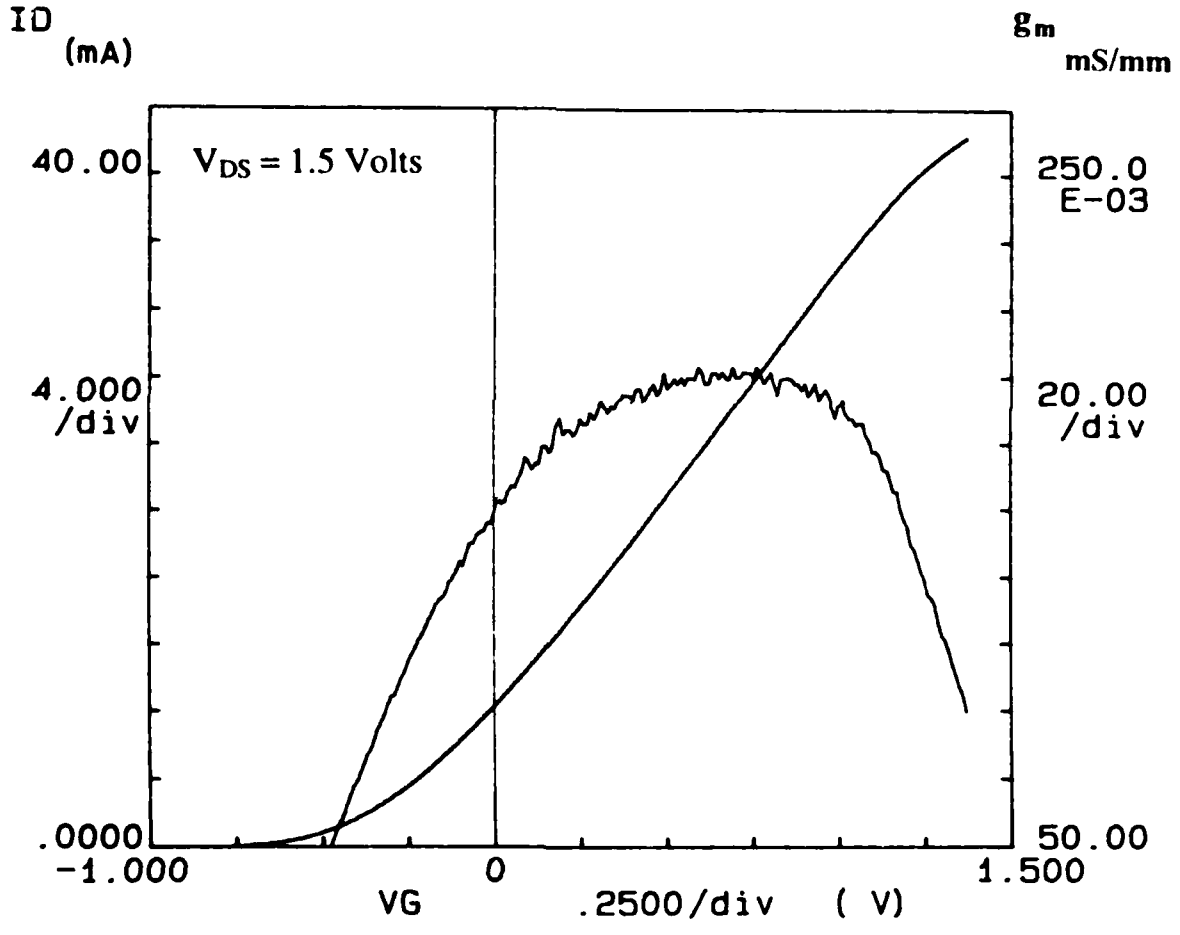


Fig. 4.4 Combined Plot of I_D vs. V_{GS} and G_m vs. V_{GS} (with V_{DS} = 1.5 V) for Sample 3379D (p^+-Graded)

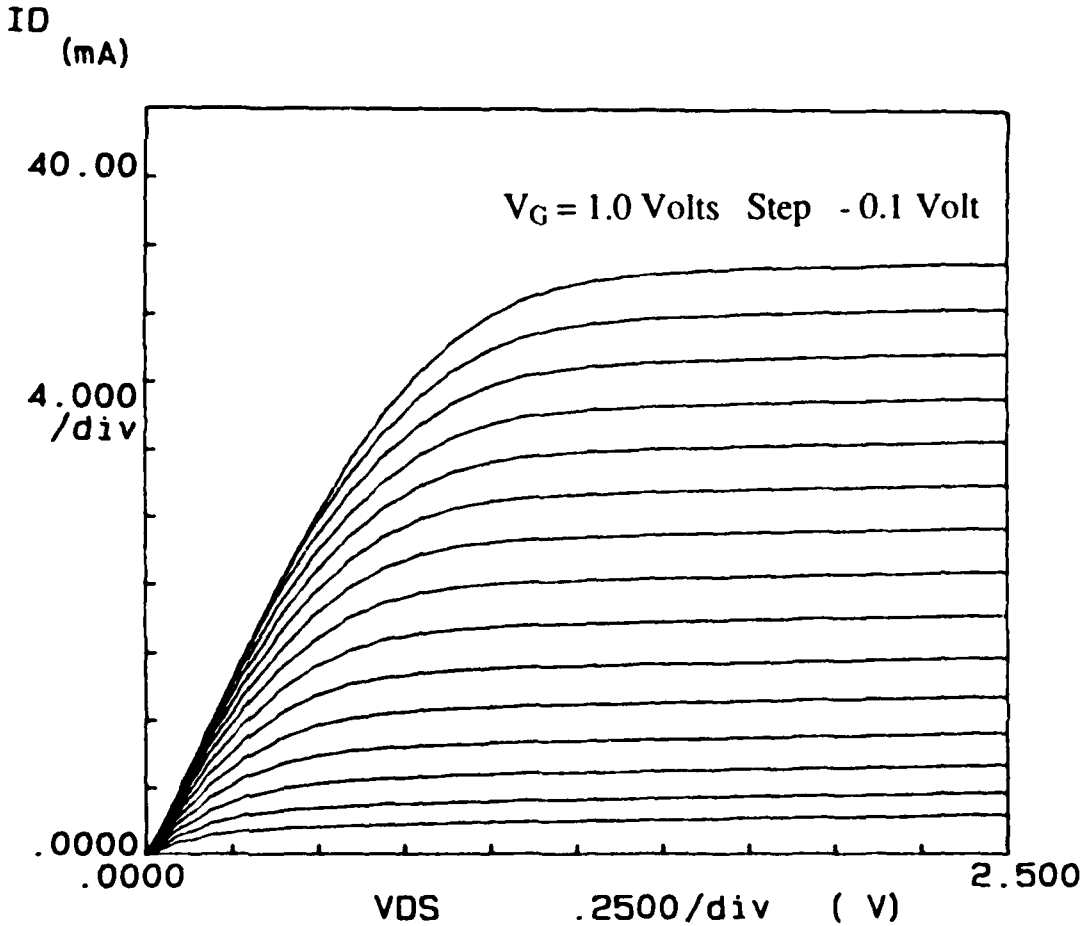


Fig. 4.5 Plot of I_D vs. V_{DS} for Sample 3379D (p^+-Graded)

Table 4.3

Summary of Measured (ESP)MODFET Effective

Schottky-Barrier Height and Threshold Voltage

Device Type	Mean Barrier Height $q\phi_B^*$ (eV)	Theoretical Model 2 $q\phi_B^*$ (eV)	Mean Threshold Voltage V_{OFF} (volts)	Theoretical Model 2 V_{OFF} (volts)
		Layer 3379		
Graded	0.89	0.8	- 0.41	- 1.25
Graded	0.92	0.8	- 0.47	- 1.25
p^+-Graded	1.61	1.63	- 0.50	- 0.52
p^+-Graded	1.54	1.63	- 0.48	- 0.52
		Layer 3381		
Graded	0.91	0.8	- 0.98	- 1.25
Graded	0.58	0.8	- 1.22	- 1.25
Graded	0.85	0.8	- 0.91	- 1.25
Graded	0.89	0.8	- 1.40	- 1.25
		Layer 3408		
Ungraded	0.70	0.8	- 0.40	- 1.25
Ungraded	N/A	0.8	N/A	- 1.25
p^+-Ungraded	0.93	1.49	- 0.55	- 0.67
p^+-Ungraded	1.49	1.49	- 0.46	- 0.67
DXL-0503	0.68	0.7	- 1.27	N/A
MPD-H503	0.68	0.7	- 1.40	N/A

Table 4.4

Summary of Measured (ESP)MODFET

Peak Transconductance (V_{DS} = 1.5 V) and Source and Contact Resistance

Device Type	Scaled g_m (mS/mm)	Scaled g_{mo} (mS/mm)	Scaled R_S (Ω-mm)	Scaled R_C (Ω-mm)
		Layer 3379		
Graded	250	448	1.77	0.15
Graded	228	364	1.64	0.2
p^+-Graded	175	209	0.94	0.14
p^+-Graded	190	226	0.83	0.13
		Layer 3381		
Graded	250	571	2.25	0.31
Graded	110	139	1.91	0.25
Graded	240	410	1.73	0.19
Graded	311	623	1.61	0.23
		Layer 3408		
Ungraded	232	355	1.49	0.23
Ungraded	N/A	N/A	N/A	N/A
p^+-Ungraded	168	188	0.62	0.09
p^+-Ungraded	195	234	0.86	0.16
DXL-0503	156	181	0.89	N/A
MPD-H503	159	223	1.81	N/A

Resistance Measurements. The results of the resistance measurements are included in Table 4.4. The contact (ohmic) resistance was measured using the transmission line method (TLM) as shown in Fig. 4.6. Sets of source-drain contact pads, separated by 2, 4, 6, and 10 microns, were located within test patterns (50 μm wide) on each sample. The samples were placed on the microprobe station connected to the HP 6181 DC current source. First, the HP 3465 multimeter was calibrated with a set of 10, 0.1 - 10 K Ω, 0.1 percent wire wound resistances (to include the resistance of the HP 3465's test leads). Then, a fixed current of 10 mA was passed through the contact pairs. The voltage drops between contacts was measured with the HP 3465 multimeter. The contact resistance was measured at low electric fields so that a constant 2DEG concentration could be assumed [46:568]. This resulted in an excellent linear fit of resistance vs. contact spacing data. The combined resistance of the two ohmic contacts and their adjoining semiconductor material was calculated using Ohm's Law. The resistances were then plotted against the contact spacings. The result was a straight line where the ordinate's intercept (contact spacing equal to zero) is twice the contact resistance ($2R_C$). Dividing R_C by two and then multiplying by the contact width gives the normalized or scaled R_C in units of Ω-mm.

Next, the source resistances (R_S) were measured by applying a fixed current (I_{GS} = 10 mA) between the gate and source, and the resultant voltage drop across the drain and source (V_{DS}) was measured as in Fig. 4.7. The source resistance is a combination of R_C plus the parasitic semiconductor resistance. Virtually all of V_{DS} is dropped across R_S and, knowing I_{GS}, one may easily calculate R_S from Ohm's law.

Microwave Characterization

Six fabricated samples with excellent DC characteristics (the best of those measured) were selected for microwave characterization (samples 3379A, 3379C, 3379D, 3381D, 3408A, and 3408D). First, overlay metallization was evaporated onto the six samples as

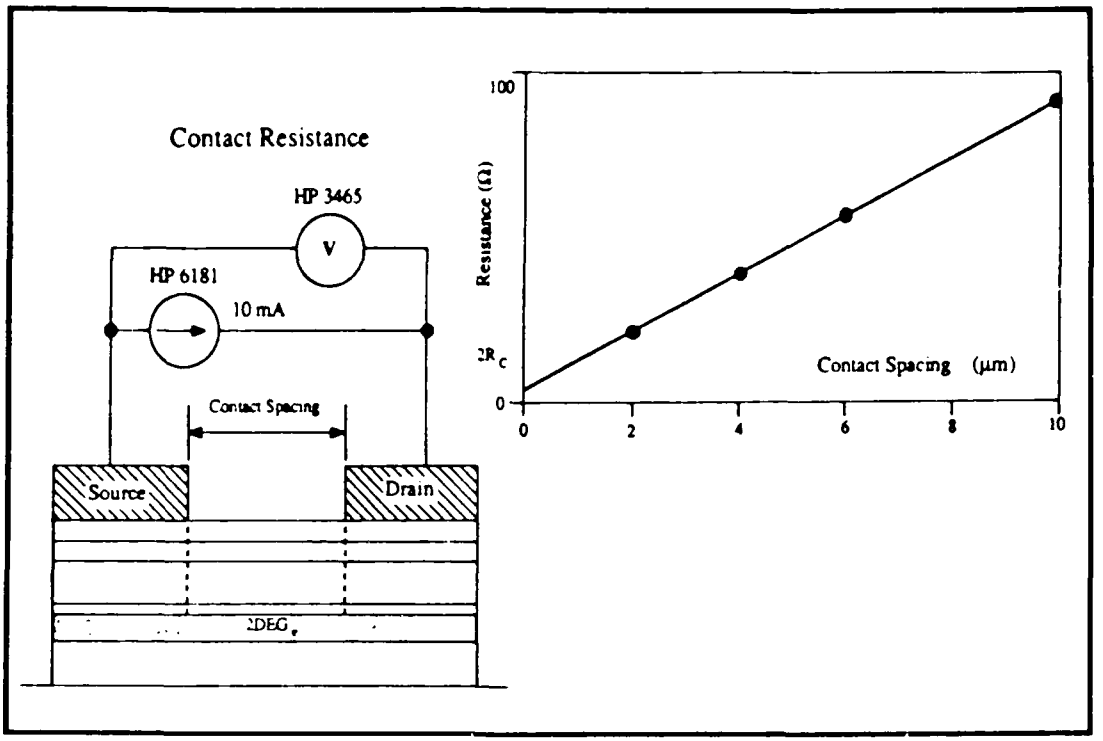


Fig. 4.6 Contact Resistance Measurement Technique

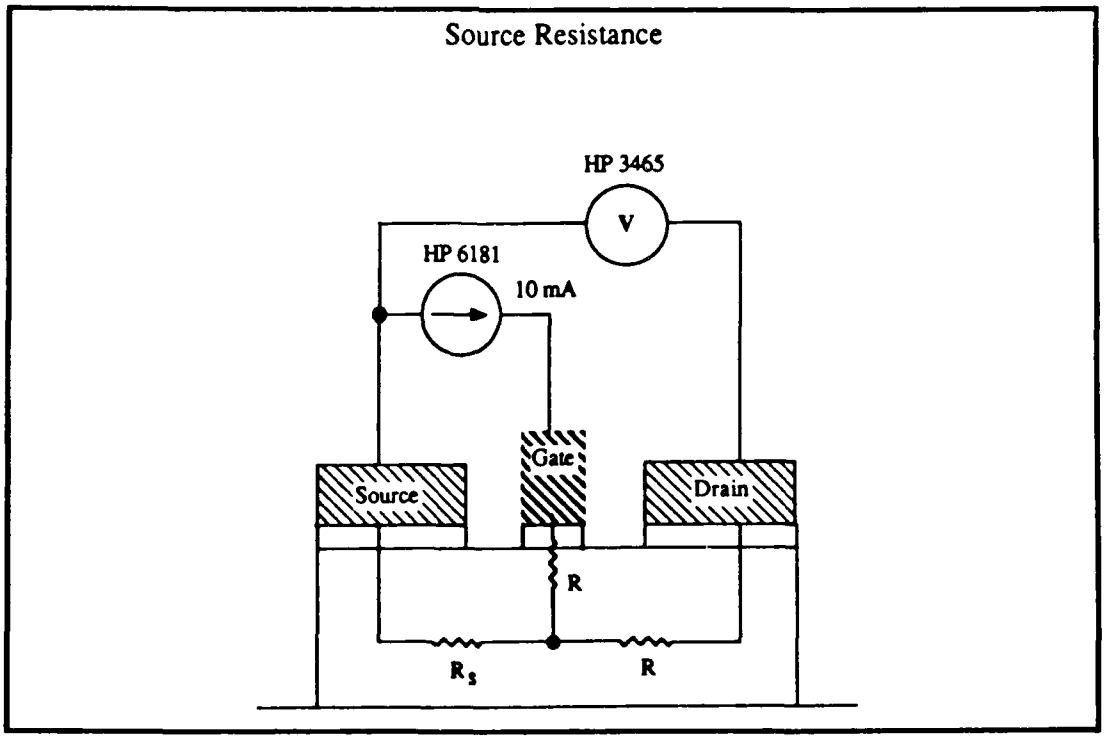


Fig. 4.7 Source Resistance Measurement Technique

described in Appendix D. The six samples were then lapped (to 250 μm), diced, and five randomly chosen MODFETs from each sample were mounted onto stripline carriers using nonconducting epoxy. The 2-port S-parameters were measured from 1 to 25 GHz for each set of MODFETs, and then used to calculate h_{21} and G_{max}. Finally, noise figure (NF) measurements were taken for the best performing MODFET from each of the six samples. As with the DC measurements, the DXL-0503 and the MPD-H503 were first characterized to verify the operation of the test equipment. All measurements were performed in the dark at about 300 °K.

S-Parameter Measurement. The S-parameters for each of the mounted MODFETs were measured using an HP 8510 Network Analyzer System [40]. The system included: an HP 8510 Network Analyzer, an HP 8515A S-Parameter Test Set, and an HP 8340B Synthesized Sweeper (10 MHz - 26.5 GHz). This network analyzer system is capable of error-corrected measurements of reflection and transmission signals. Calibration and device measurements were performed using a matched set of two test port return cables (HP 85131B cable set). First, all connectors (including those on the microstripline test fixture) were cleaned using compressed air and freon-treated foam-tipped swabs as outlined in [40: 28-34]. Next, the HP 85052A calibration kit was used to perform a full 2-port measurement calibration [40:198-199]. The following standards were used: a shielded open, a short, a 50 Ω load, and a thru. A computer algorithm was used to store "Full 2-Port Model" error correction information at each calibrated frequency. This provided full error correction of source match, reflection and transmission signal path frequency response, load match, and isolation for S_{11}, S_{21}, S_{12}, and S_{22} [40:198]. Next, four stripline carrier standards (as above), mounted on stripline carriers identical to those of the mounted MODFETs, were used to re-calibrate the HP 8510. The stripline carrier standards were sequentially mounted onto the microstripline test fixture. The calibration proceeded exactly as before.

The S-parameters (corrected by HP developed software algorithms) were then measured from 1 to 25 GHz at 1 GHz intervals for the mounted MODFETs of this study. The DC bias was adjusted to maximize the MODFET's gain. The measured S-parameters were stored on magnetic disk for further analysis. An example set of measured S-parameters for sample 3379C is shown in Table 4.5.

Forward Current Gain and Maximum Available Power Gain. The forward current gain (h_{21}) and the maximum available power gain (G_{max}) were calculated from the measured S-parameters using (2.10) and (2.11). The magnitudes of h_{21} and G_{max} (expressed in dB) were plotted against the log of frequency for each MODFET as shown in Fig. 4.8. A representative plot of G_{max} (dB) and $20\log|h_{21}|$ (dB) versus the log of frequency for several MODFET samples may be found in Appendix E. The plotted values of G_{max} and $|h_{21}|$ were extrapolated at - 6 dB/octave down to 0 dB in order to determine the unity current gain frequency (f_T where $|h_{21}| = 1$ or 0 dB) and the maximum frequency of oscillation (f_{max} where $G_{max} = 1$ or 0 dB). The extrapolated values of f_T and f_{max} for the six MODFET samples are listed in Table 4.6.

Noise Figure. The MODFET noise figures (NFs) were measured using an HP 8970A noise figure meter and measurement system as shown in Fig. 4.9. The results are listed in Table 4.7. The system included a standard noise source (HP 346B) and an external local oscillator (HP 8341A) (0.01 to 20 GHz). First, the system was run through a standard calibration at 4, 8, and 12 GHz. The MODFET (mounted on a stripline carrier) was placed in its test fixture and connected between the noise source and the input to the noise figure meter. The MODFET's DC bias was supplied by an external power supply through bias network connectors (HP 11590A). The frequency of the local oscillator was manually adjusted to 4, 8, and 12 GHz. The noise source injects a known amount of noise at a given frequency into the MODFET. Noise is internally generated in the MODFET and adds to this

Table 4.5

Measured S-Parameters for Sample 3379C (p^+-Graded)

Freq	S11		S21		S12		S22		S21
GHZ	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang	dB
1.00000	0.992	-15.2	3.922	168.1	0.016	80.8	0.773	-4.8	11.87
2.00000	0.970	-29.9	3.783	156.6	0.031	72.1	0.758	-9.3	11.56
3.00000	0.940	-43.6	3.582	145.9	0.043	64.2	0.736	-13.3	11.08
4.00000	0.905	-56.1	3.348	136.2	0.054	57.2	0.712	-16.6	10.50
5.00000	0.870	-67.2	3.107	127.4	0.062	51.1	0.688	-19.5	9.85
6.00000	0.838	-77.2	2.874	119.5	0.069	45.9	0.666	-21.8	9.17
7.00000	0.809	-86.0	2.658	112.3	0.074	41.6	0.646	-23.8	8.49
8.00000	0.784	-93.8	2.463	105.9	0.078	37.8	0.630	-25.6	7.83
9.00000	0.763	-100.8	2.288	100.0	0.081	34.6	0.616	-27.2	7.19
10.00000	0.746	-107.0	2.132	94.5	0.083	31.9	0.604	-28.7	6.58
11.00000	0.731	-112.5	1.994	89.4	0.085	29.6	0.595	-30.1	5.99
12.00000	0.718	-117.4	1.871	84.7	0.086	27.5	0.587	-31.5	5.44
13.00000	0.708	-121.9	1.762	80.2	0.087	25.8	0.581	-32.9	4.92
14.00000	0.699	-126.0	1.664	76.0	0.088	24.3	0.575	-34.3	4.42
15.00000	0.692	-129.7	1.577	71.9	0.088	22.9	0.571	-35.7	3.96
16.00000	0.686	-133.0	1.498	68.0	0.088	21.8	0.568	-37.1	3.51
17.00000	0.681	-136.1	1.427	64.3	0.088	20.8	0.565	-38.5	3.09
18.00000	0.677	-139.0	1.363	60.7	0.088	19.9	0.563	-40.0	2.69
19.00000	0.673	-141.7	1.304	57.2	0.088	19.2	0.562	-41.5	2.31
20.00000	0.670	-144.1	1.250	53.8	0.088	18.5	0.561	-43.0	1.94
21.00000	0.668	-146.5	1.201	50.6	0.088	18.0	0.560	-44.5	1.59
22.00000	0.666	-148.6	1.156	47.3	0.087	17.5	0.560	-46.1	1.26
23.00000	0.664	-150.7	1.114	44.2	0.087	17.2	0.560	-47.7	0.93
24.00000	0.663	-152.6	1.074	41.1	0.086	16.9	0.560	-49.3	0.62
25.00000	0.662	-154.4	1.038	38.1	0.086	16.7	0.561	-50.9	0.32

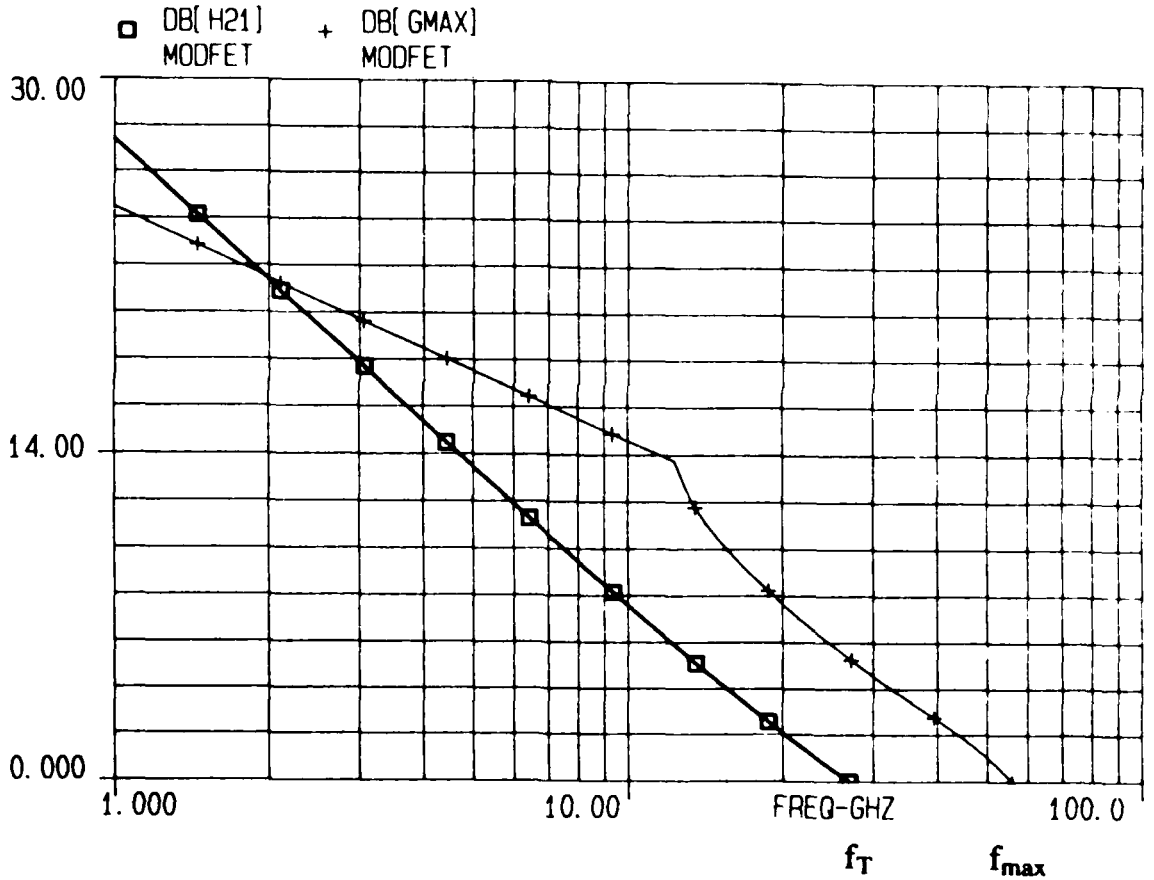


Fig. 4.8 Plot of the Maximum Available Gain (G_{max}) and Forward Current Gain ($20\log|h_{21}|$) vs. Frequency for Sample 3379D (p^+-Graded)

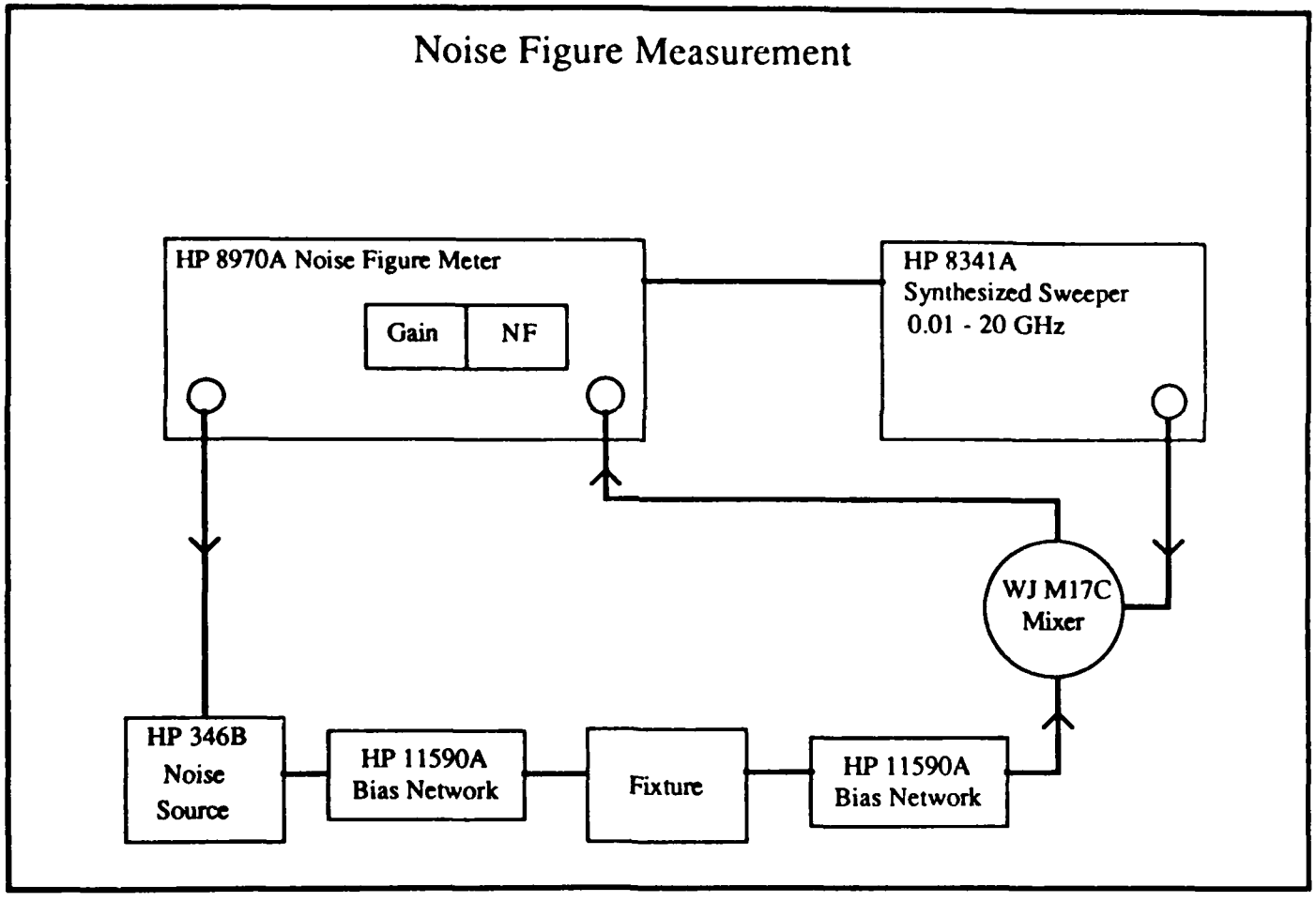


Fig. 4.9 Noise Figure Measurement Technique

Table 4.6

Extrapolated Values of f_T and f_{max}

Sample	Type	Mean f_T (GHz)	Range f_T (GHz)	Mean f_{max} (GHz)	Range f_{max} (GHz)
3379A	Graded	19	17 to 22	26.5	26 to 30
3379C	p^+-Graded	23.5	20.5 to 24	48	39.5 to 49
3379D	p^+-Graded	26	22 to 27	54	53 to 55.5
3381D	Graded	23.5	19 to 30.5	33.5	32 to 41
3408A	Ungraded	16	13.5 to 19.5	22	19.5 to 23
3408D	p^+-Ungraded	24.5	21.5 to 26.5	40.5	38 to 41.5
DXL-0503	N/A	39	N/A	82	N/A
MPD-H503	N/A	50	N/A	110	N/A

Table 4.7

Summary of (ESP)MODFET Noise Figure Measurements

NF and (Associated Gain) Values all in dB

Sample	Type	4 GHz	8 GHz	12 GHz
3379A	Graded	1.6 (13.2)	1.8 (9.4)	1.9 (5.2)
3379C	p^+-Graded	1.2 (12.3)	1.5 (10.3)	1.7 (5.2)
3379D	p^+-Graded	2.1 (13.5)	2.4 (10.0)	2.9 (5.9)
3381D	Graded	1.9 (17.1)	2.3 (11.1)	2.8 (8.8)
3408A	Ungraded	2.3 (15.3)	2.5 (7.4)	3.3 (4.3)
3408D	p^+-Ungraded	1.8 (15.0)	2.2 (9.4)	2.9 (5.7)

known input noise. The noise figure meter, after calibration, analyzes this change in noise level and the NF in dB, along with the associated gain in dB, is instantaneously displayed on the meter's front panel. The applied DC bias was adjusted until the minimum NF was obtained. Also, insulated metal chips (metchips) were placed on the input and output striplines of the stripline carrier and moved back and forth in order to adjust the input and output impedances. In addition to the DC bias, the metchips were adjusted until the lowest NF was obtained.

V. Analysis of Results

This chapter analyzes the experimental procedures and measured results of Chapter IV. It also examines the merits of the previously derived first-order charge-control models (Models 1 and 2) by comparing them to two general purpose modulation-doped heterostructure models. In this chapter, the measured values of the effective Schottky-barrier height (ϕ_B*) and other characteristics of the (ESP)MODFET will be compared to theory and their merits will be analyzed. This chapter is divided into four main sections. First, the (ESP)MODFET's DC performance is evaluated. Second, the (ESP)MODFET's microwave performance is evaluated. Third, the merits of the derived first-order charge-control models (Models 1 and 2) are discussed. The models are compared to a quantum mechanical model developed at The University of Michigan [42]. Models 1 and 2 are also compared to a numerical "classical" charge-control model (Model 3) developed by the author. Model 3 was developed to overcome some of the short-comings of the original models. Model 3 accounts for free holes and free electrons in the (ESP)MODFET structures (Models 1 and 2 do not account for free charge) and yields a more accurate energy band diagram for a given heterostructure. Finally, the effect of the fabrication procedures on the measured *MODFET* performance is discussed.

MODFET DC Performance

Effective Schottky-Barrier Height. It has been shown for the first time that the effective Schottky-barrier height ($q\phi_B$* in units of eV) of strained channel MODFETs may be enhanced (increased). Combined plots of I_G vs. V_{GS} (gate diode curve) (with $V_{DS} = 0$) for MODFET samples 3379A (graded) and 3379D (p^+-graded), and MODFET samples 3408A (ungraded) and 3408D (p^+-ungraded), are shown in Figs 5.1a and 5.1b,

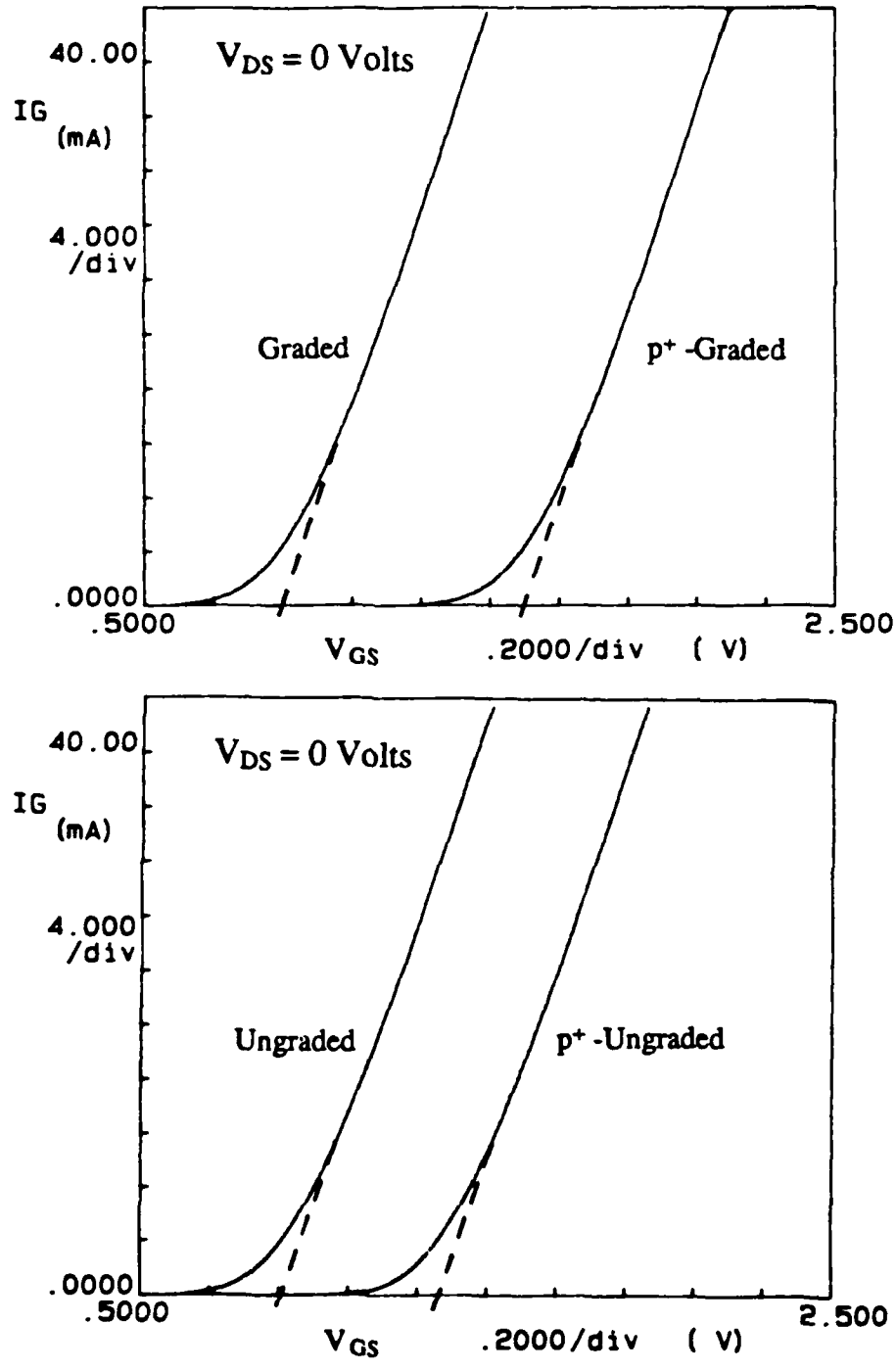


Fig. 5.1 Comparison of the Effective Schottky-Barrier Height of (a) Samples 3379A (Graded) and 3379D (p^+-Graded), and (b) Samples 3408A (Ungraded) and 3408D (p^+-Ungraded).

respectively. The effective Schottky-barrier height ($q\phi_B^*$) was increased from about 0.9 eV to 1.6 eV for the graded samples by the addition of the p^+-GaAs surface epitaxial layer. Similarly, the effective Schottky-barrier height for the ungraded samples increased from about 0.8 eV to 1.5 eV. The general trend was an increase in the effective Schottky-barrier height of about 0.7 eV for both the graded and ungraded n-$Al_xGa_{1-x}As$ barrier layer MODFETs. The Schottky-barrier height of the graded (no p^+-GaAs) samples 3381A through D was between 0.85 - 0.95 eV. This is higher than the expected Schottky-barrier height of Al on n-GaAs of 0.80 eV [89:291]. However, the Schottky-barrier was formed on the graded samples between an Al /$Al_{0.3}Ga_{0.7}As$ interface, and in fact, the Schottky-barrier height for the graded samples without p^+-GaAs epitaxial layers were consistently about 0.9 eV (except for sample 3381B). The Schottky-barrier height for the ungraded sample 3408A was closer to 0.8 eV. A variation in ϕ_B (and ϕ_B^*) between and within samples is not unexpected since the graded $Al_xGa_{1-x}As$ barrier epitaxial layer has a rapidly decreasing mole fraction beyond the Al/$Al_xGa_{1-x}As$ interface. In fact, the AlAs mole fraction (as theoretically designed) would change from 0.30 down to 0.15 in 100 Å, or in less than 37 monolayers of atoms.

Another possible explanation for the Schottky-barrier height variation was graphically illustrated in Fig. 3.8. Here it was shown how a modest change in the p^+-GaAs epitaxial layer doping density (or thickness) can have a dramatic effect upon ϕ_B^*. For the MODFET structures in this study, MBE was used to grow the "layers" and a high degree of epitaxial layer design accuracy (on the atomic level) was expected. However, the MODFETs were fabricated by wet chemical etching, notably the step using a 3:1:150 $NH_4OH:H_2O_2$:DIW etchant to selectively remove the p^+-GaAs. Thus incomplete p^+-GaAs epitaxial layer removal during fabrication or nonlinear grading of the $Al_xGa_{1-x}As$ barrier layer could make it difficult to measure consistent values for ϕ_B (or ϕ_B^*). Because a limited number of

samples were available for this work, statistical trends could not be established (with a high degree of certainty).

Threshold Voltage. The threshold voltage (V_{OFF}), like ϕ_B*, is strongly dependent on the thicknesses and doping densities of the n-$Al_xGa_{1-x}As$ and p^+-GaAs epitaxial layers. To a lesser degree, V_{OFF} is also dependent on the grading scheme of any of the doped layers and the thickness of the $Al_{0.15}Ga_{0.85}As$ separation layer. An interesting observation can be made from Table 4.3. The value of V_{OFF} was found to increase (become less negative) for sample 3379 when the p^+-GaAs was removed beneath the gate. For example, V_{OFF} for etched sample 3379A was about 0.1 eV less negative than for enhanced Schottky-barrier sample 3379D. A similar trend was found for ungraded sample 3408. A more negative shift in V_{OFF} was expected. When the p^+-GaAs epitaxial layer is removed, the ionized donor electrons in the $Al_xGa_{1-x}As$ barrier now move to lower states in the Al Schottky-barrier gate metal. The electrons also diffuse into the strained channel layer as before, though now in greater quantity. This can be verified by examining the V_{OFF} of sample 3381 (about -1.0 to -1.4 volts) which initially did not contain a p^+-GaAs epitaxial layer (the charge-control models also predict this). Even if the p^+-GaAs was not completely etched, a negative shift in V_{OFF} would still be expected. It is discounted that the p^+-GaAs under the gate (and the parasitic p^+-GaAs between gate and source, and gate and drain) was not etched at all since the measured results indicate reduced Schottky-barriers for control samples in addition to high current I_D vs. V_{DS} curves for both control and enhanced samples. It is possible that the p^+-GaAs was overetched, removing part of the n-$Al_xGa_{1-x}As$ barrier epitaxial layer. This would increase V_{OFF} toward zero, making the MODFET more enhancement mode. For example, Model 2 predicts a V_{OFF} = - 0.46 volts for sample 3381 if the top 100 Å of the n-$Al_xGa_{1-x}As$ barrier epitaxial layer was removed.

Transconductance. The measured transconductances (g_m) were shown in Table 4.4. The g_m of the enhanced Schottky-barrier samples was expected to decrease since the term

"d_{eff}" increases in (2.5) with the added 100 Å p^+-GaAs epitaxial layer. The g_m was expected to decrease by roughly 19 percent (e.g. d_{eff} increased from 430 Å to 530 Å assuming Δd = 50 Å in (2.5)). As shown in Table 4.4 , the g_m decreased by about 15 - 30 percent.

The measured g_m (scaled to units of mS/mm) for sample 3381D (311 mS/mm) is the highest reported to date for an $In_yGa_{1-y}As/Al_xGa_{1-x}As$ pseudomorphic MODFET with y = 0.15 and a gate- length (L_G) of 1 μm (the value reported in the literature was 270 mS/mm [46]). A scanning electron microscope was used to determine L_G. The gate length of the fabricated devices was found to be consistently 1.2 μm.

Contact and Source Resistance. The measured contact (R_C) and source (R_S) resistances (scaled to units of Ω-mm) were shown in Table 4.4. The n-type ohmic contacts on samples 3379A through D (p^+) and 3408C through D (p^+) were alloyed through a p^+-GaAs epitaxial surface layer. The ohmic contacts on the remaining samples were alloyed through the $n\text{-}Al_xGa_{1-x}As$ barrier layers. The measured values of R_C (scaled) spanned 0.09 to 0.31 Ω -mm, with slightly larger values measured for the unenhanced Schottky-barrier samples. The variation in R_C was expected because a manually operated alloying furnace was used. A typical R_C (scaled) value of 0.17 Ω-mm has been reported [46:568] for pseudomorphic MODFETs. The value of the large-signal source resistance (R_S) is a function of the 2DEG concentration. Thus, R_S is related to V_{OFF}. As V_{OFF} becomes more negative (for a depletion mode device), R_S should decrease. However, the values of R_S (scaled) varied between 0.62 - 2.25 Ω-mm and did not correspond to the expected theoretical R_S decrease with decreasing V_{OFF}. This corresponds to the possibility of overetching of the $n\text{-}Al_xGa_{1-x}As$ barrier layers and to the variation in R_C. A typical value of 2.7 Ω-mm has been reported [46:568] for pseudomorphic MODFETs with a source-to-drain separation of 3 μm.

MODFET Microwave Performance

Unity Current Gain Frequency and Maximum Frequency of Oscillation. The extrapolated values of f_T and f_{max} were listed in Table 4.6. The previously reported values for f_T and f_{max} were 21.5 GHz and 37.0 GHz, respectively [46:569]. The values of f_T and f_{max} were higher for the enhanced Schottky-barrier samples in both the graded and ungraded cases. However, since the low-frequency transconductances were lower, the gain of the enhanced Schottky-barrier samples was lower at the lower frequencies. The extrapolated values of f_T and f_{max} were 26 GHz and 54 GHz, respectively, for the p^+-graded sample. This is an improvement over the previously reported values for InGaAs/AlGaAs pseudomorphic MODFETs of similar gate geometries.

Microwave Modelling. The measured S-parameters for each of the MODFET structures fabricated in this study were used to develop small-signal equivalent circuit models (as in Fig. 2.18). The measured S-parameters were loaded into an HP 9133 computer equipped with a software program called Touchstone™ (version 1.5) [92]. Starting with an initial estimate and range for each element and the equivalent small-signal circuit model of Fig. 2.18, an optimization algorithm (least squares) was run until the measured S-parameters were closely matched (within 0.5 percent). The results are shown in Table 5.1. Critical observation of Table 5.1 (see also Table 2.2) shows that the parasitic gate resistance (R_g), the gate to source capacitance (C_{gs}), and the low-frequency intrinsic transconductance (g_{mo}) were smaller for the p^+-graded Schottky-barrier samples, compared to their graded (unenhanced) control samples.

Noise Figure. The measured noise figures (NF) for the MODFET structures of this study should be treated only as preliminary values. A trend could not be established from the results because the measured values varied beyond the expected experimental error (± 0.1 dB at 12 GHz). Additionally, the limited number of fabricated devices made it difficult to analyze the results with a high degree of certainty. As shown in Table 4.7, the

Table 5.1

Equivalent Small-Signal Circuit Parameters

Parameter	Sample						Unit
	3379A	3379C	3379D	3381D	3408A	3408D	
	Device Type						
	Graded	p^+-Graded	p^+-Graded	Graded	Ungraded	p^+-Ungraded	
g_{mo}	79.98	51.17	59.35	88.4	69.92	65.44	mS
τ	4.14	4.13	4.19	4.11	4.77	4.85	psec
C_{gs}	0.54	0.37	0.35	0.48	0.69	0.49	pF
C_{dg}	35.87	27.09	28.13	32.82	40.23	31.28	fF
C_{ds}	63.12	41.2	39.98	66.2	78.24	59.9	fF
G_d	2.70	2.86	2.68	3.08	2.67	2.81	mS
R_i	2.06	1.31	1.49	1.20	1.79	3.67	Ω
R_g	15.61	6.01	5.55	10.05	12.2	4.31	Ω
R_d	7.43	7.20	6.10	6.22	7.03	9.53	Ω
R_s	2.22	2.31	2.10	3.29	3.76	5.78	Ω
L_g	23.13	21.87	20.34	22.89	19.41	17.97	pH
L_d	19.90	31.23	33.60	33.20	27.77	27.85	pH
L_s	9.97	13.23	10.10	11.11	15.78	13.34	pH
f_T	22	21	26	30.5	16	24	GHz
f_{max}	28	44	54	41	22	40	GHz

NF's of the identical samples 3379C and 3379D were considerably different. It is believed that the test equipment induced an error of at least 0.5 dB into the measurements, because

of the difficulty in manually sweeping the frequency of the local oscillator and externally DC biasing the device under test. The values of NF above 4 GHz for 1 μm gate length pseudomorphic MODFETs have not been previously published. The NF of the MPD-H503 HEMT is reported to be 0.4, 0.8, and 1.2 dB at 4, 8, and 12 GHz respectively [87]. Considering that this device has a gate length of 0.5 μm, the values measured in this study are not unreasonable (see (2.15)).

Charge-Control Models

Models 1 and 2. The first-order charge-control Models 1 and 2 that were derived in Appendices A and B, respectively, yielded a good quantitative picture of the expected energy band diagram for a given MODFET structure. Also, the models produced good estimates for the values of n_s (verified in the next sub-section) and V_{OFF}, given an initial Schottky-barrier height (ϕ_B). As was shown in Fig. 3.10, the $q\phi_B$* of samples 3379C and D, and of samples 3408C and D was expected to be (see Table 3.3) 1.63 and 1.49 eV, respectively. The measured $q\phi_B$* of the samples (see Table 4.3) was 1.61 and 1.51 eV, respectively. The models gave a good picture of the effect of varying the p^+-GaAs epitaxial layer's doping density or thickness, and also of the effect of varying the linear grading scheme of the AlAs mole fraction. Originally, the n-$Al_xGa_{1-x}As$ barrier layer was to be doped at 3×10^{18} cm^{-3}, corresponding to the pseudomorphic MODFETs fabricated by Ketterson et. al [46]. It was also desired to keep all device dimensions unchanged so a comparison could be made. However, the recessing of the n-$Al_xGa_{1-x}As$ barrier layer could not be performed since a p^+-GaAs was grown on top of this layer. Model 2 was used to plot the energy band diagram of this structure (same as Fig. 3.6 only with $N_D = 3 \times 10^{18}$ cm^{-3}). The resulting energy band diagram revealed that the conduction band would dip below and then abov · the Fermi energy level, in addition to the dip of the quantum-well. This would result in a large population of quantum-confined electrons in part of the n-$Al_{0.15}Ga_{0.85}As$ barrier layer. This would essentially form a parasitic MESFET

path since the effective mobility of electrons is greatly reduced here (e.g. the ionized donors preserve coulombic scattering, defeating the purpose of modulation-doping). This will be elaborated on in the next sub-section. When the thickness of the n-$Al_{0.15}Ga_{0.85}As$ was reduced, Model 2 showed that the ϕ_B* would drastically be reduced. The compromise design of this work allowed both enhanced and unenhanced samples to be grown at identical thicknesses and doping densities, while avoiding the problem stated above.

Classical and Quantum Mechanical Models. The quantum mechanical charge-control model recently developed by Jaffe [44] at The University of Michigan was used to evaluate the two models developed in Appendices A and B. The model uses a numerical technique to self-consistently solve Poisson's and Schrödinger's equations. The result is energy band, eigenfunction, and charge distribution diagrams for a given MODFET structure. The details of the model are described in Appendix F.

Using the quantum mechanical model, the energy band diagram of samples 3379C and D was determined and is shown in Fig. 5.2. The straight-lines within the well correspond to the allowed energy levels (eigenenergies). The quantum confined charge was taken to be restricted between z = 300 to 900 Å (an assumption). The distribution of quantum confined charge was determined from the eigenfunctions (ψ_i) corresponding to the allowed energy levels. The corresponding eigenfunctions for the first six sub-bands are shown plotted in Fig. 5.3. The quantum confined charge density of the i^{th} sub-band at a distance z from the gate ($\rho_i(z)$) is found from

$$\rho_i(z) = n_i \psi_i^*(z)\psi_i(z) \quad (cm^{-3}) \tag{5.1}$$

where $\psi_i^*(z)\psi_i(z)$ is the normalized probability of electron occupancy and n_i is the density of electrons in the i^{th} sub-band. The charge distribution diagram for samples 3379C and D is shown in Fig. 5.4. This figure contains the doping densities of the epitaxial layers

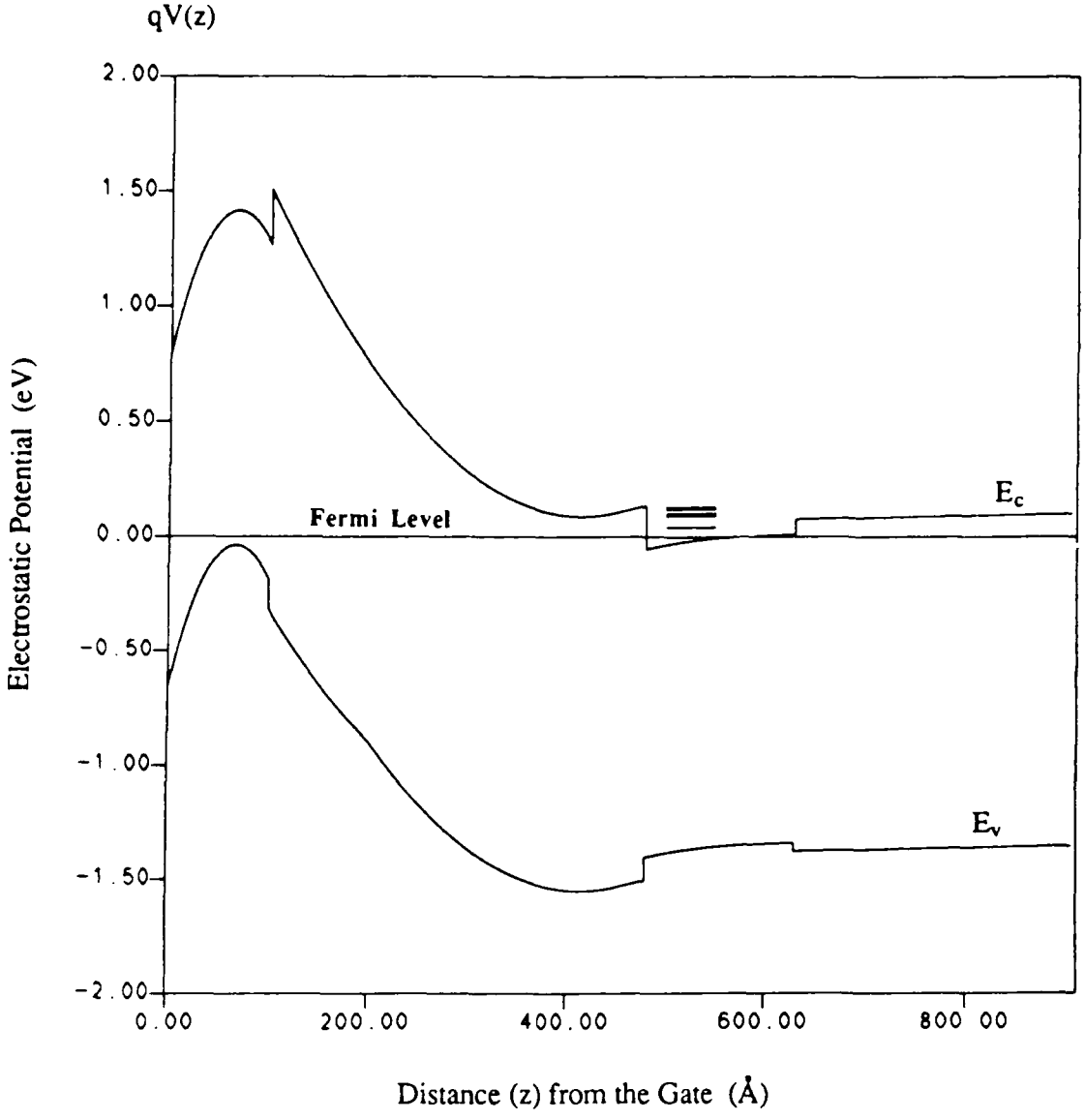


Fig. 5.2 Energy Band Diagram of Samples 3379C and D as Calculated from the Quantum Mechanical Model ($V_G = 0$). The Fermi Energy Level is Taken as a Zero Reference for the Conduction (E_c) and Valence (E_v) Bands. The Lines Within the Well Represent the Allowed Energy Levels of the Quantum Confined Electrons [42]

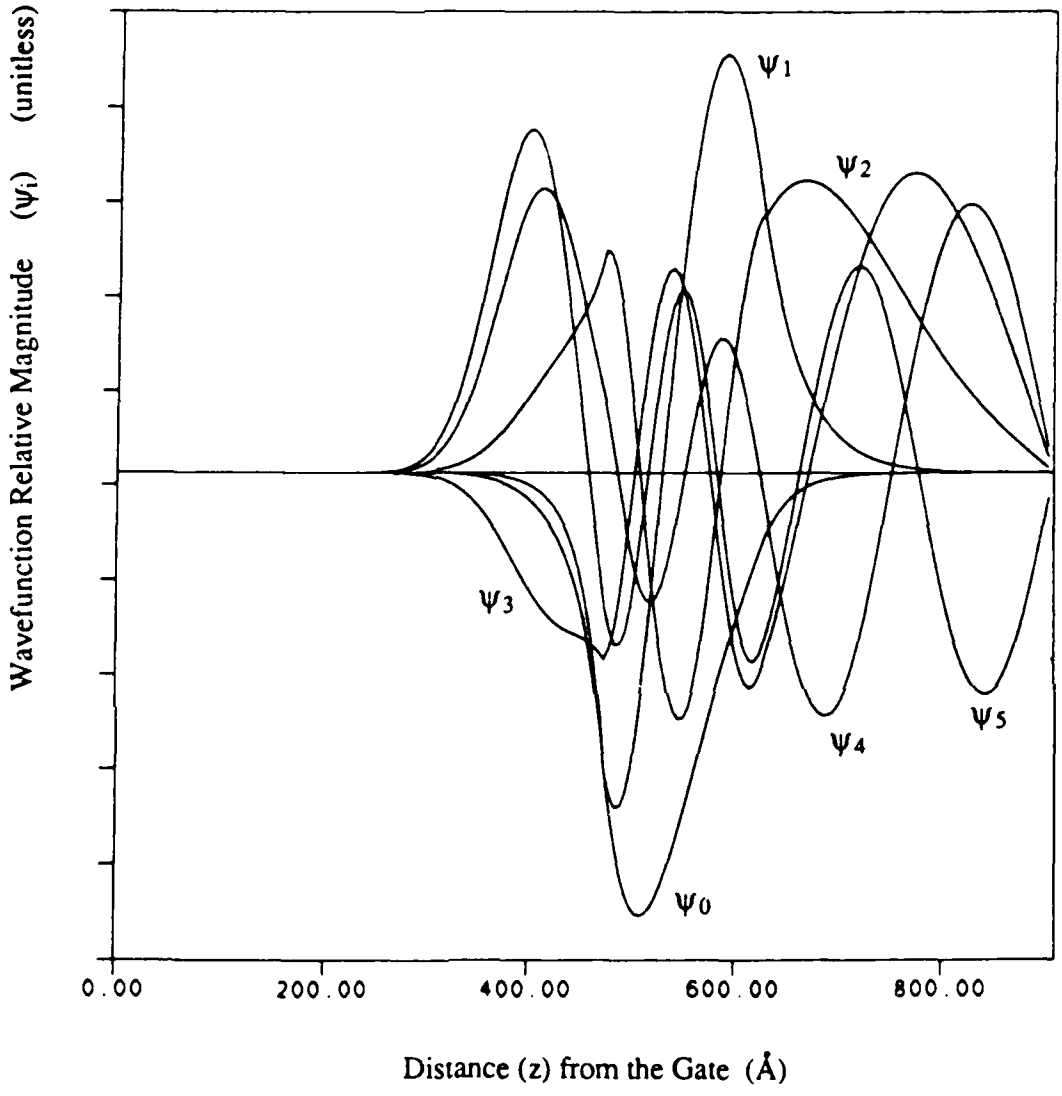


Fig. 5.3 Wavefunctions Corresponding to the Allowed Energy Levels of Fig. 5.2 for Samples 3379C and D [42]

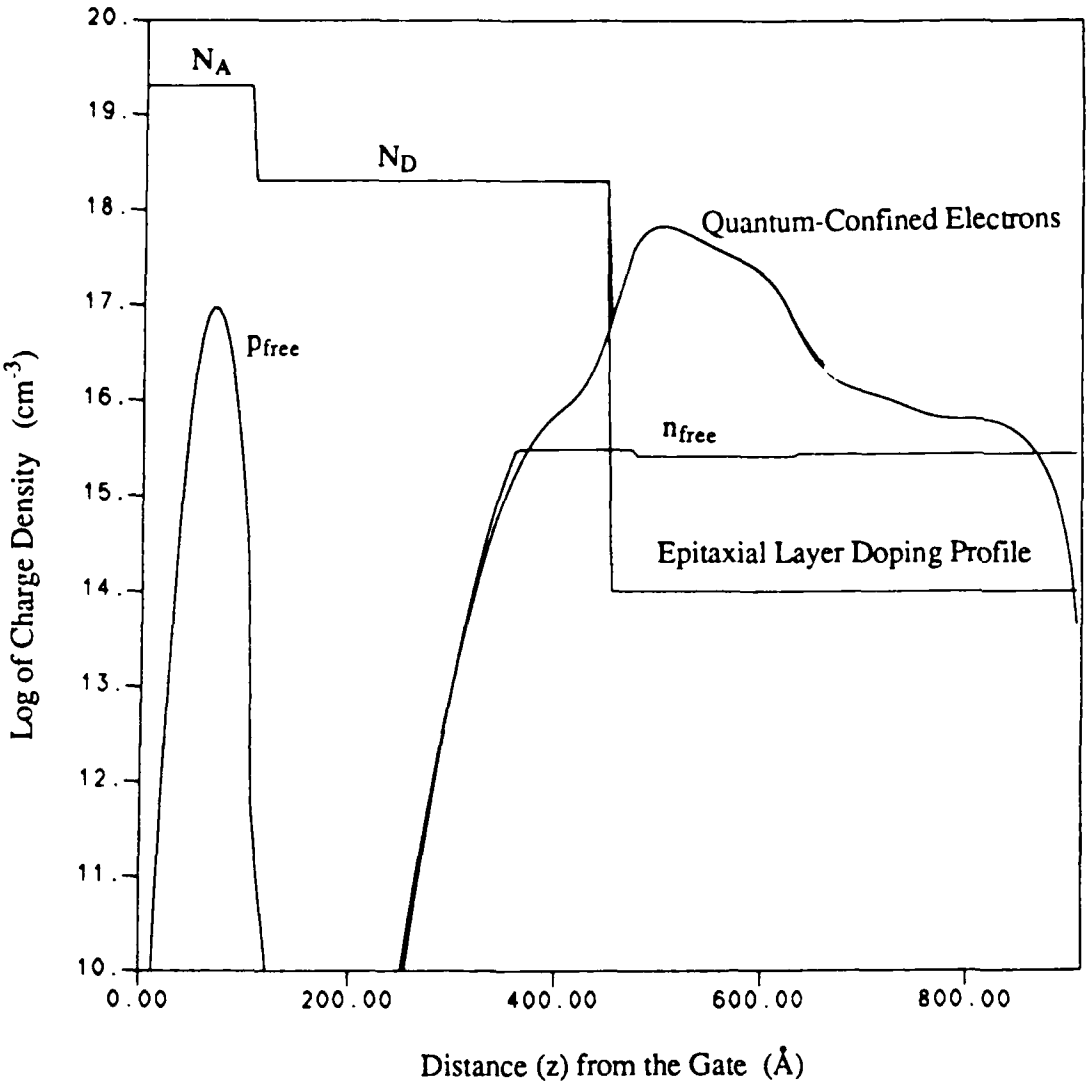


Fig. 5.4 Charge Distribution Diagram for Samples 3379C and D as Calculated from the Quantum Mechanical Model. The Densities of Free Holes and Free Electrons are shown, along with the Doping Densities of the Epitaxial Layers and the Distributed Density of the Quantum Confined Charge [42]

($|N_D-N_A|$), of the free electrons ($|n_{free}|$) and holes (p_{free}), and of the quantum-confined electrons. Initially, Jaffe's model treats the quantum-confined charge as if it were free charge governed by Fermi-Dirac statistics (called a "classical" solution). Poisson's equation is solved and the resulting energy band diagram is almost identical to that of the quantum model. This initial classical solution is then used as the starting point for the self-consistent solution which includes quantum-confined charge. The difference in the two models is illustrated by comparing their charge distribution diagrams. The charge distribution diagram for the classical solution (samples 3379C and D) is shown in Fig. 5.5. It can be seen, by comparing Fig. 5.4 with Fig. 5.5, that the "classical" solution to Poisson's equation is an excellent approximation to the more exact quantum mechanical solution.

From the eigenfunctions in Fig. 5.3, it is seen that not all of the quantum-confined electrons are within the quantum-potential well. This is partially due to the probability of barrier penetration inherent in the eigenfunctions, but it is mainly due to shape of the conduction band near the well, and the fact that Schrödinger's equation was applied between z = 300 to 900 Å (assumed wavefunction boundaries). Table 5.2 lists the values of the energy levels (referenced to the Fermi level = 0), the total quantum-confined charge in each level, the quantum-confined charge within the well at each level, and the fraction of the confined charge that is within the well. Also shown is the case for a quantum well of thickness 200 Å. The value predicted for n_s (quantum-confined charge in the well) is about 5.971×10^{11} cm^{-2} for the 150 Å well and about 6.215×10^{11} cm^{-2} for the 200 Å well (this is a 3.9 percent difference). The well size of 150 Å was originally chosen to insure that the pseudomorphic approximation would hold. The value of n_s predicted by Model 2 was 6.44×10^{11} cm^{-2}. However, it must be remembered that Model 2 treats n_s as an infinitesimally thin sheet charge and does not consider the distributed free charge (n_{free}). From Fig. 5.2 an effective Schottky-barrier height ($q\phi_B^*$) of about 1.5 eV is expected, compared to a $q\phi_B^*$ 1.63 eV predicted by Model 2. The measured value of $q\phi_B^*$ = 1.63 eV

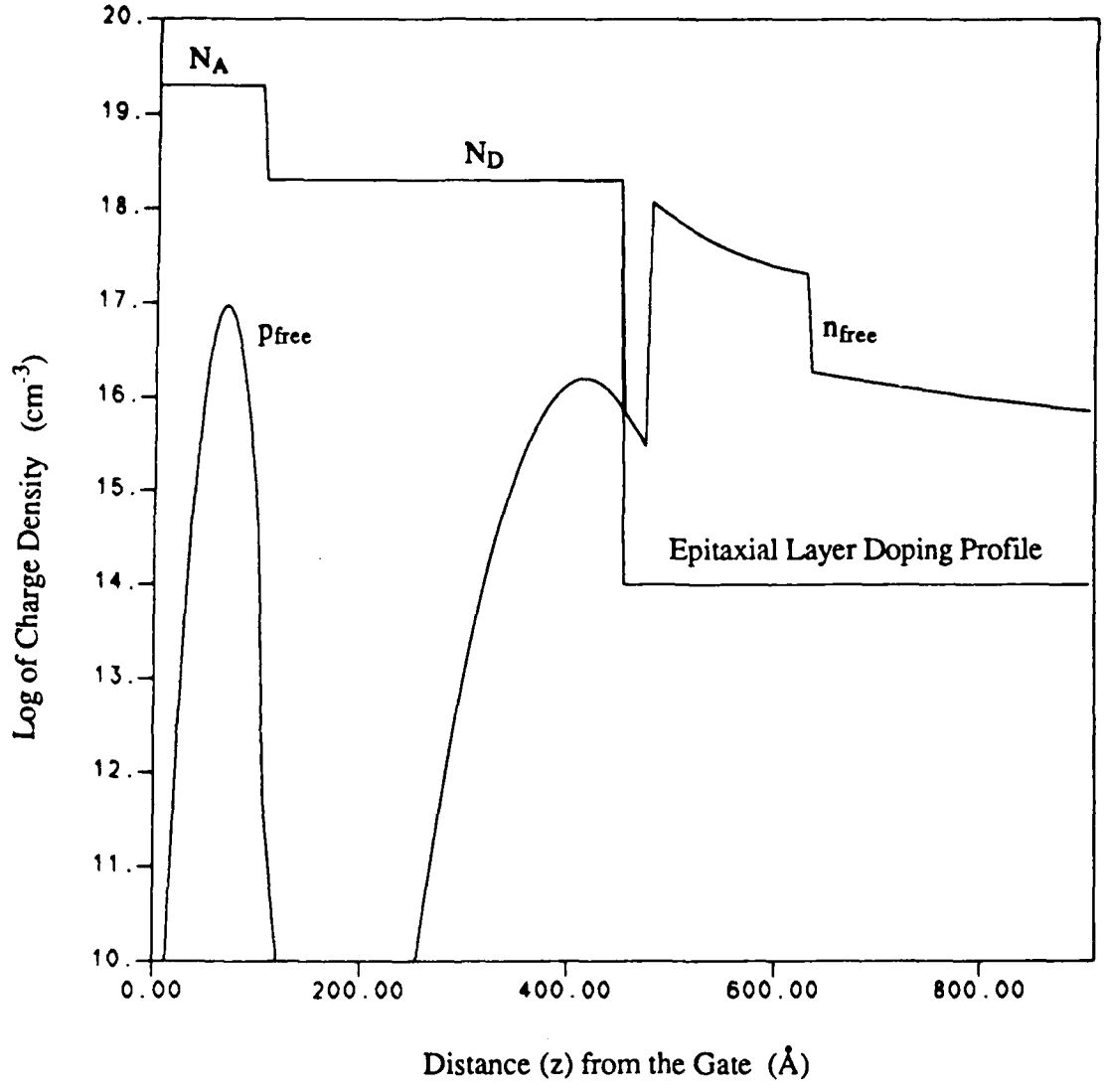


Fig. 5.5 Charge Distribution Diagram for Samples 3379C and D as Calculated from the Classical Model. The Densities of Free Holes and Free Electrons are shown, along with the Doping Densities of the Epitaxial Layers and the Distributed Density of the Quantum Confined Charge [42]

Table 5.2

Calculated Values of the Energy Levels (E_n) (Referenced to the Fermi Level = 0), the Total Quantum-Confined Charge in Each Level (Q_n), the Quantum-Confined Charge Within the Well at Each Level (Q_n in Well), and the Percent of the Confined Charge that is Within the Well at Each Level for Layer 3379. The Values were Obtained from the Quantum Mechanical Charge-Control Model [42]

Strained Channel Thickness = 150 Å

Sub-band Number	E_n	Q_n	Q_n in Well	Fraction Q_n in Well
0	- 4.18883E-03	5.32499E+11	4.81830E+11	0.90485
1	4.02905E-02	1.31492E+11	1.08086E+11	0.82200
2	8.91543E-02	1.85590E+10	4.98743E+09	0.26873
3	1.01443E-01	6.20511E+09	1.24196E+09	0.20015
4	1.17824E-01	4.98890E+09	3.63677E+08	0.07290
5	1.28651E-01	3.82386E+09	6.36503E+08	0.16646

Total Sheet Charge = 6.97568E+11

Total Free Charge = 6.46569E+10

Fraction of Quantum Confined Charge in Well = 0.8560

Strained Channel Thickness = 200 Å

Sub-band Number	E_n	Q_n	Q_n in Well	Fraction Q_n in Well
0	- 1.57036E-03	4.95856E+11	4.49664E+11	0.90684
1	3.51166E-02	1.56291E+11	1.41980E+11	0.90843
2	7.45010E-02	3.70866E+10	2.77249E+10	0.74757
3	1.07084E-01	4.31821E+09	5.46019E+08	0.12645
4	1.18559E-01	5.52948E+09	1.03682E+09	0.18751
5	1.32144E-01	2.97696E+09	5.75718E+08	0.19339

Total Sheet Charge = 7.02059E+11

Total Free Charge = 5.91585E+10

Fraction of Quantum Confined Charge in Well = 0.8853

could be obtained in the quantum model by setting $q\phi_B$ equal to 0.9 eV (measured value), rather than 0.8 eV as in Fig. 5.2.

The quantum confinement of charge outside the quantum well can be illustrated by letting $N_D = 3 \times 10^{18}$ cm^{-3} in the structure of samples 3379C and D. Using this value for N_D, the energy band and charge distribution diagrams were plotted (using the quantum mechanical model) and are shown in Figs 5.6 and 5.7, respectively. It can be seen that a substantial number of confined electrons exist in the conduction band of the n-$Al_{0.15}Ga_{0.85}As$ barrier epitaxial layer. Model 2 also predicts that the conduction band will dip below the Fermi level for this structure. However, it does not account for the resultant quantum-confined or free electron charge. Even in the "classical" case, the Fermi-Dirac statistics would predict a large population of free electrons when $E_F - E_c > 0$.

For this reason, a revised classical charge-control model (Model 3) was developed. The model accounts for free charge and, as shown above, should be an excellent approximation to the exact quantum mechanical solution. Model 3 uses a numerical solution to the one-dimensional Poisson equation along with the Maxwell-Boltzmann approximation to the Fermi-Dirac distribution function. The details of Model 3 are contained in Appendix F. Model 3 was used to plot the energy band and charge distribution diagrams for the MODFET samples fabricated in this work in order to predict the effective Schottky-barrier height of these devices. The diagrams for samples 3379C and D, 3379A and B and 3381A through D, and 3408C and D are presented in Figs 5.8, 5.9, and 5.10, respectively. Comparing Fig. 5.8 with Figs 5.2 and 5.5, differences in the plotted values of n_{free}, p_{free} etc. are noticeable. This is mainly due to the different semiconductor parameter values used by the two models. The values used for the permittivities (ε) and bandgaps (E_g) differ the most. For example, the E_g of GaAs was taken as 1.43 eV by Jaffe, compared to 1.424 eV in Model 3. Also, the bandgap of the strained InGaAs was calculated by a tight-binding model by Jaffe, and by the equations presented in Chapter 3 (see Fig. 3.5) for Model 3. In

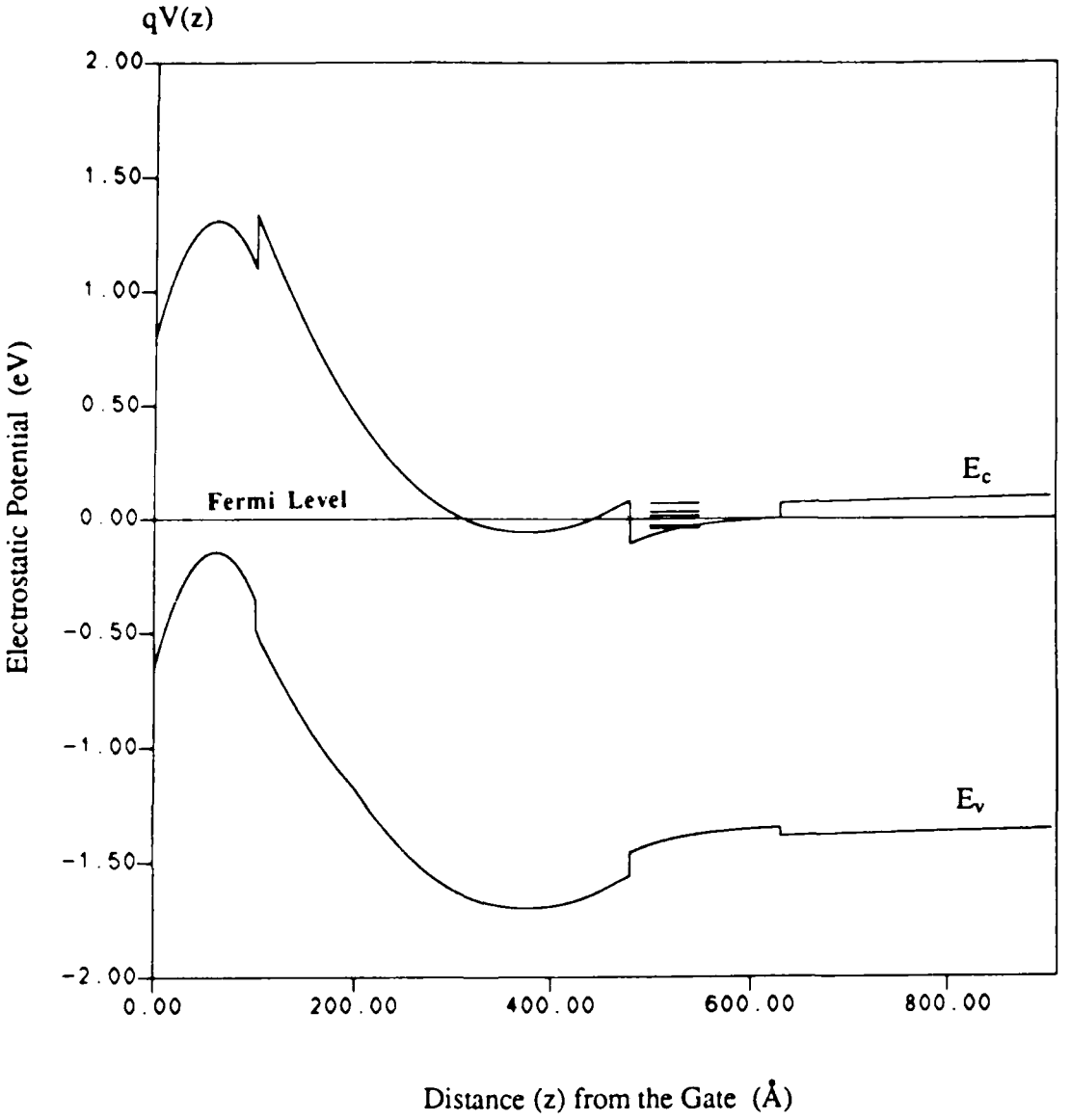


Fig. 5.6 Energy Band Diagram of Samples 3379C and D with $N_D = 3 \times 10^{18}$ cm^{-3} as Calculated from the Quantum Mechanical Model ($V_G = 0$). The Fermi Energy Level is Taken as a Zero Reference for the Conduction (E_c) and Valence (E_v) Bands. The Lines Within the Well Represent the Allowed Energy Levels of the Quantum Confined Electrons [42]

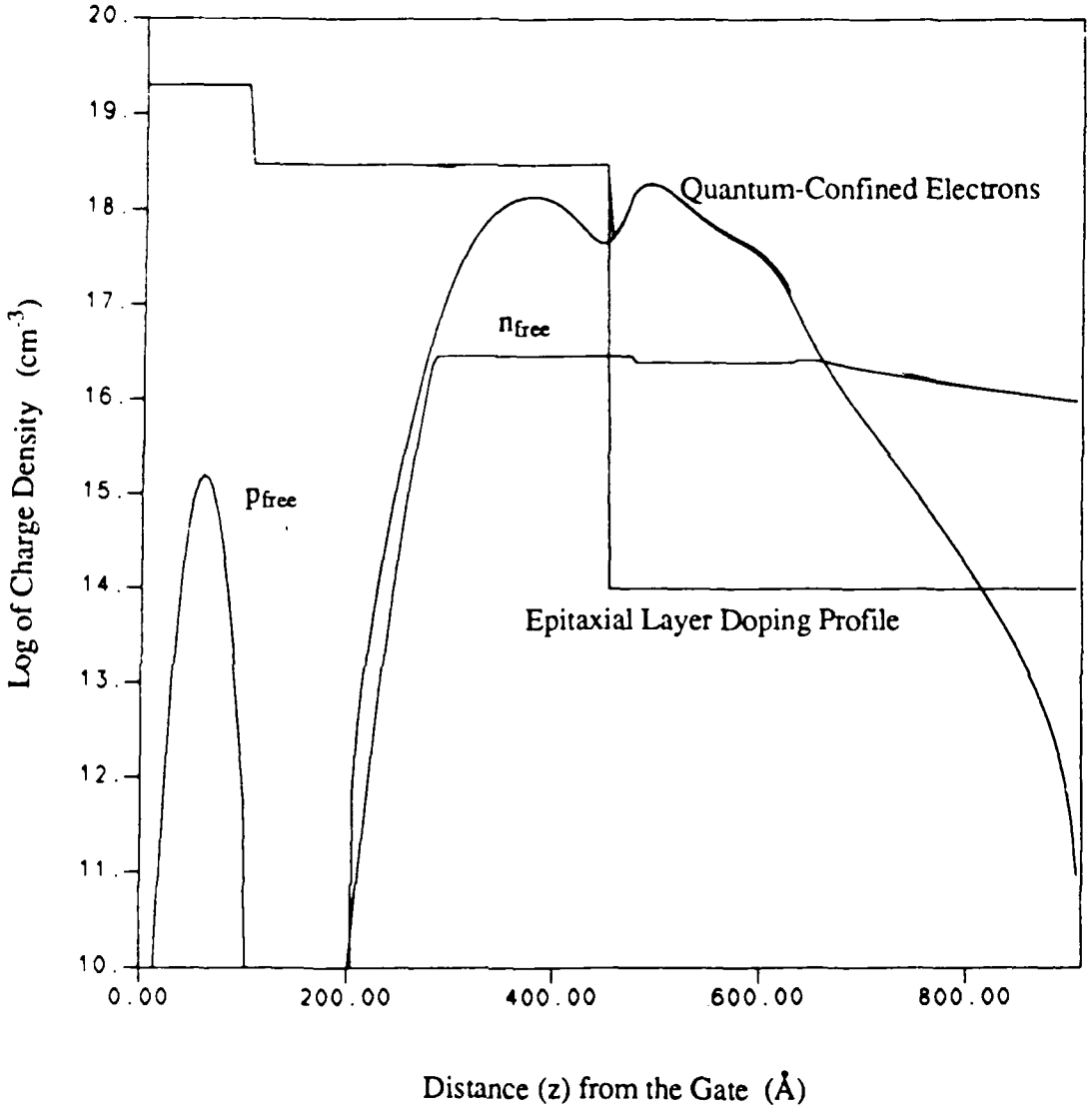


Fig. 5.7 Charge Distribution Diagram for Samples 3379C and D with $N_D = 3 \times 10^{18}$ cm^{-3} as Calculated from the Quantum Mechanical Model. The Densities of Free Holes and Free Electrons are shown, along with the Doping Densities of the Epitaxial Layers and the Distributed Density of the Quantum Confined Charge [42]

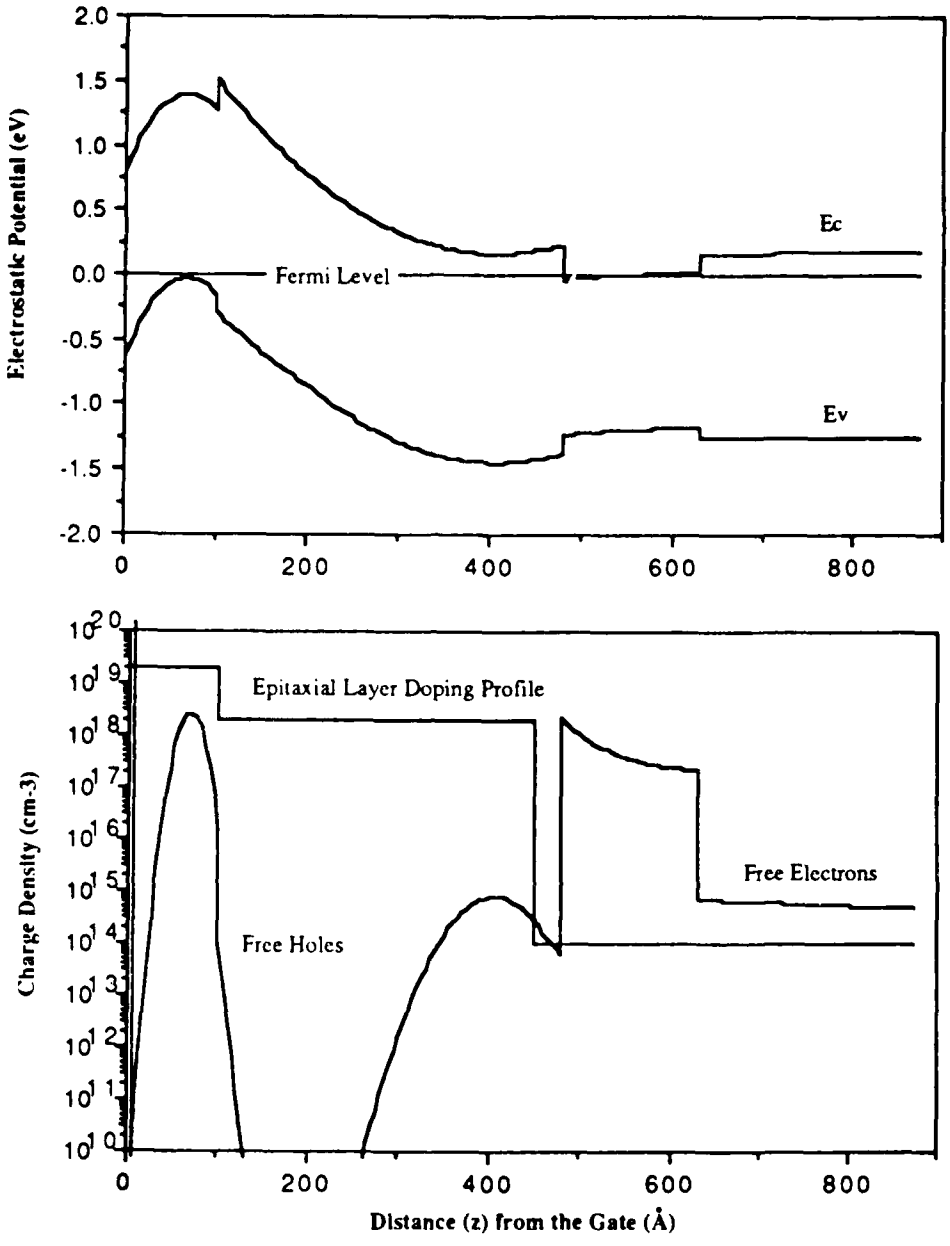


Fig. 5.8 Energy Band and Charge Distribution Diagrams for Samples 3379C and D as Calculated from Model 3 ($V_G = 0$). The Fermi Energy Level is Taken as a Zero Reference for the Conduction (E_c) and Valence (E_v) Bands. The Densities of Free Holes and Free Electrons are shown, along with the Doping Densities of the Epitaxial Layers

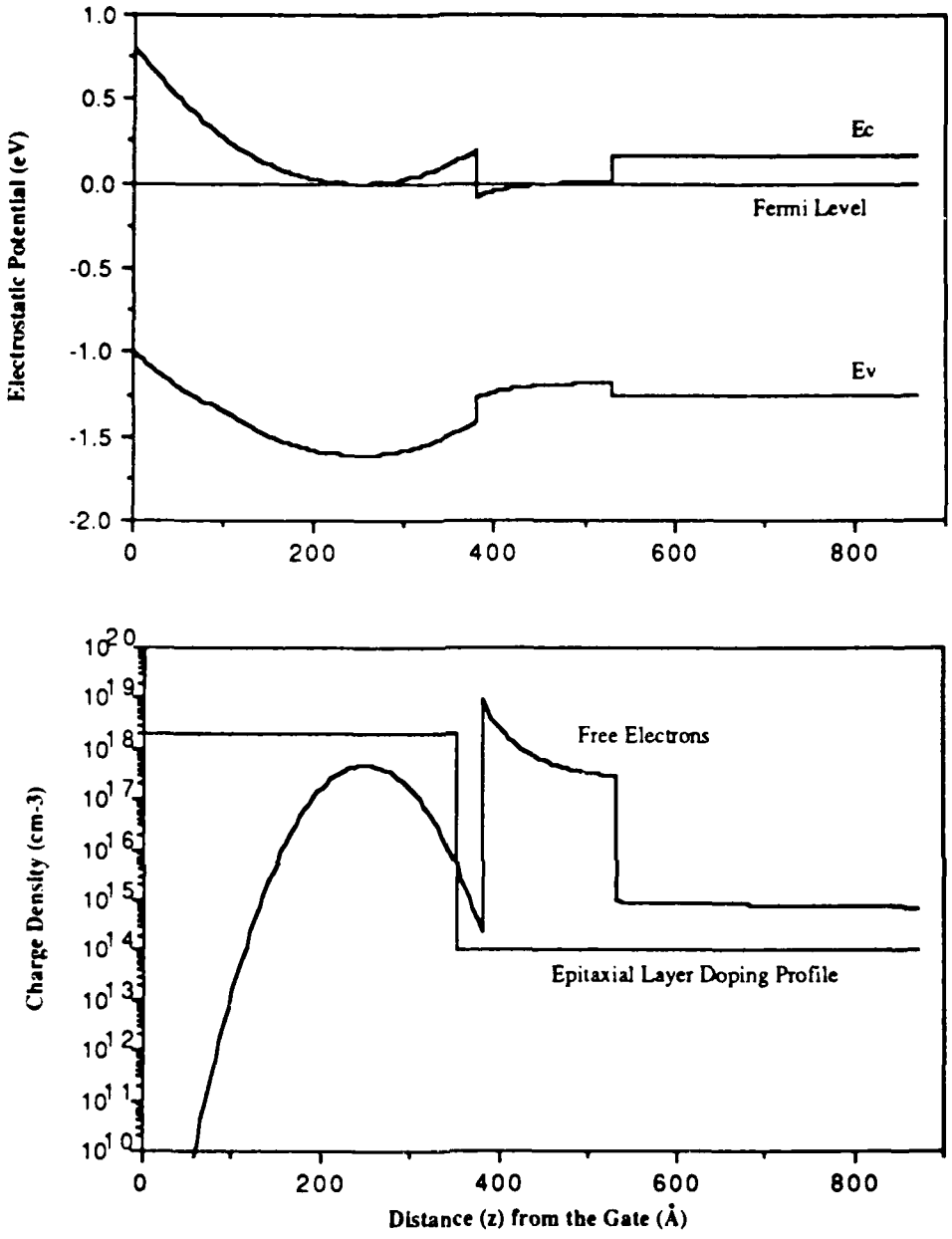


Fig. 5.9 Energy Band and Charge Distribution Diagrams for Samples 3379A and B and 3381A through D as Calculated from Model 3 ($V_G = 0$). The Fermi Energy Level is Taken as a Zero Reference for the Conduction (E_c) and Valence (E_v) Bands. The Densities of Free Holes (off the scale in this case) and Free Electrons are shown, along with the Doping Densities of the Epitaxial Layers

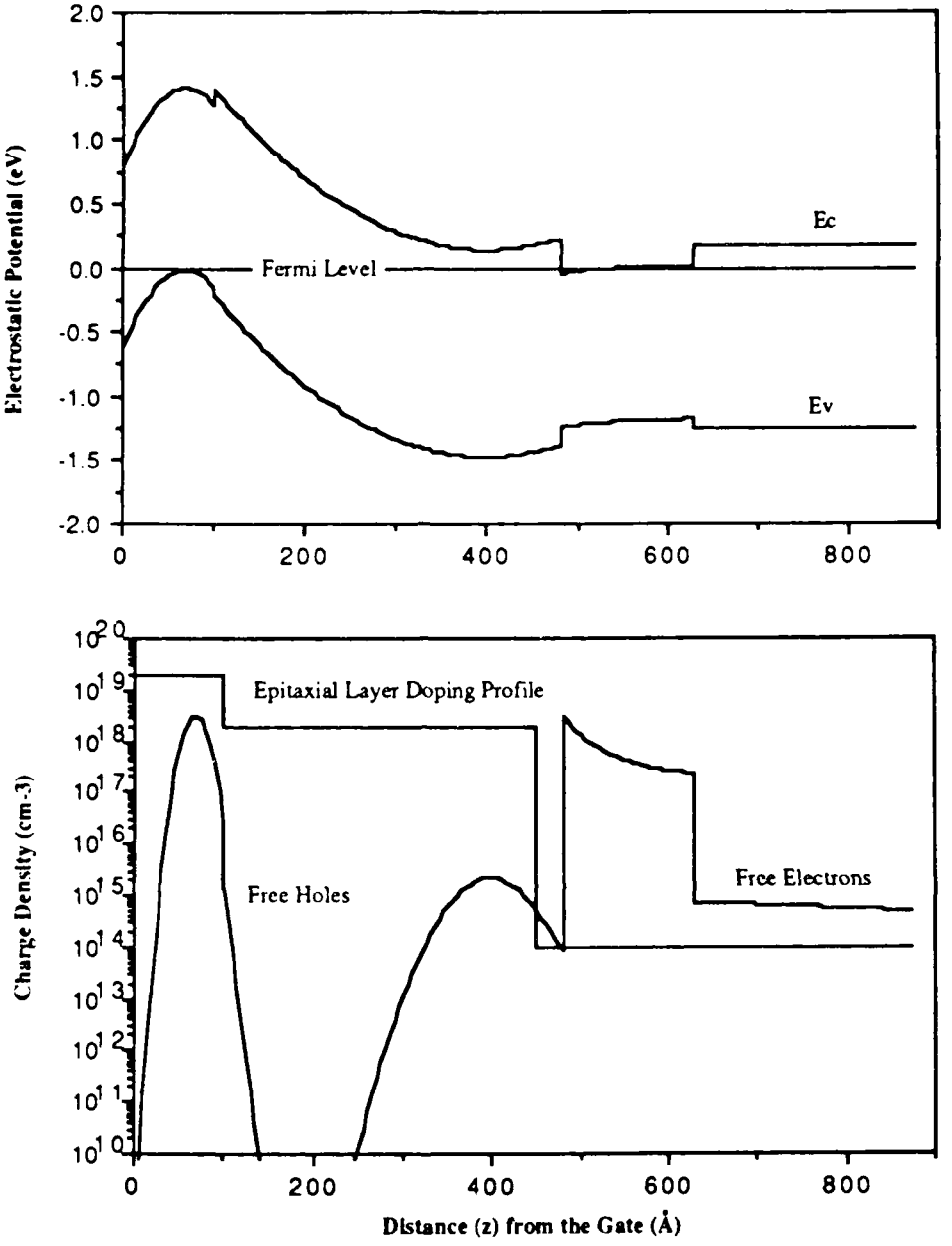


Fig. 5.10 Energy Band and Charge Distribution Diagrams for Samples 3408C and D as Calculated from Model 3 ($V_G = 0$). The Fermi Energy Level is Taken as a Zero Reference for the Conduction (E_c) and Valence (E_v) Bands. The Densities of Free Holes and Free Electrons are shown, along with the Doping Densities of the Epitaxial Layers

both cases, the 65:35 rule was used [42] to determine ΔE_c and ΔE_v, and both models show a similar ϕ_B* for samples 3379C and D. Model 3 does not calculate a value for n_s and V_{OFF} as do Models 1 and 2. The measured and modelled values of ϕ_B* are shown in Table 5.3.

Fabrication Procedures

The fabrication methodology has a strong impact on the MODFET's performance. The fabrication procedures used to fabricate the MODFETs of this study were based on those developed over many years at the University of Illinois. The only new fabrication step involved the etching of the p^+-GaAs epitaxial layer. The thrust of this thesis was to theoretically design and characterize the enhanced Schottky-barrier strained channel MODFET. Since the structure is a variation of a well researched device, each step of the fabrication was not analyzed. The measured DC and microwave performance of the MODFETs indicate that the starting MBE-grown layers were of high quality. Also, the experimental results indicate that the pseudomorphic approximation for the strained InGaAs channel epitaxial layer was valid. The etch rate and selectivity of the GaAs etchant $NH_4OH:H_2O_2$:DIW (3:1:150 by volume) needs further study.

Table 5.3

Comparison of Measured and Modelled Effective Schottky-Barrier Height (eV)

Device Type	Model 1	Model 2	Model 3	Quantum Model	Measured
p^+-Graded	1.63	1.63	1.51	1.5	1.54 to 1.61
Graded	0.8	0.8	0.8	0.8	0.85 to 0.92
p^+-Ungraded	1.45	1.46	1.4	1.4	1.43 to 1.51
Ungraded	0.8	0.8	0.8	0.8	0.63 to 0.81

VI. Conclusions and Recommendations

The purpose of this thesis was to characterize the DC and microwave performance of enhanced Schottky-barrier InGaAs/$Al_xGa_{1-x}As$ strained channel MODFETs. A notable improvement in the performance of the pseudomorphic MODFET was obtained by altering the device's material structure. In this final chapter, a list of conclusions is presented that summarize the results of this study. Additionally, a list of recommendations is given. The recommendations are proposals for further research.

Conclusions

1. The effective Schottky-barrier height (ϕ_B*) of the InGaAs/$Al_xGa_{1-x}As$ pseudomorphic MODFET may be enhanced (increased) by a p^+-GaAs surface layer.

2. The enhanced Schottky-barrier MODFETs at room temperature exhibited extremely high extrinsic transconductances (g_m); as high as 195 mS/mm. A g_m as high as 311 mS/mm was found for an unenhanced sample. This is the highest g_m reported to date for an $In_yGa_{1-y}As/Al_xGa_{1-x}As$ pseudomorphic MODFET with y = 0.15 and L_G = 1.2 μm.

3. The samples exhibited low ohmic contact resistance (R_C) with and without the p^+-GaAs epitaxial layers. The values of R_C (scaled to units of Ω-mm) varied between 0.09 to 0.31 Ω-mm, which is close to the typical value of 0.17 Ω-mm reported in the literature.

4. The sample source resistance (R_S) (scaled to units of Ω-mm) varied between 0.62 to 2.25 Ω-mm, which is lower than the typical value of 2.7 Ω-mm reported in the literature for 3 μm (drain-to-source distance) MODFETs.

5. The enhanced Schottky-barrier MODFETs with graded n-$Al_xGa_{1-x}As$ barrier epitaxial layers exhibited a unity current gain frequency (f_T) and a maximum frequency of

oscillation (f_{max}) as high as 27 and 59 GHz, respectively. This is an improvement over the previously reported values of 21.5 and 37 GHz, respectively, and is a result of lower parasitic gate resistance and lower gate-to-source capacitance as predicted by circuit modelling.

6. The enhanced Schottky-barrier MODFETs with graded barrier layers had slightly lower noise figures than the unenhanced Schottky-barrier MODFETs with graded barrier layers. A NF of 1.7 dB at 12 GHz was measured for an enhanced sample, compared to 1.9 dB for the unenhanced sample. The NF measurements should be treated as preliminary values.

7. The first-order charge-control models (Models 1, 2 and 3) provide an accurate quantitative description of the effective Schottky-barrier height (within 0.1 eV) for a given MODFET structure, as verified by DC measurements.

Recommendations

1. Use the quantum mechanical charge-control model (or Model 3) to optimize the enhanced Schottky-barrier MODFET structure for the highest f_{max} and lowest NF possible. The design used in this work was a compromise design so that both enhanced and unenhanced MODFETs could be fabricated (with identical thicknesses and doping densities) and compared. For example, a higher g_m and n_s could be attained by decreasing the thickness of the n-$Al_xGa_{1-x}As$ barrier layer while increasing its doping density to 3×10^{18} cm^{-3}. Increasing n_s will also reduce R_S. Also, an intrinsic surface layer could be used in place of the p^+-GaAs epitaxial layer to reduce gate leakage current. A different $Al_xGa_{1-x}As$ grading scheme should be studied.

2. Perform a further analysis and optimization of the fabrication procedures to improve the MODFETs performance. This should include: optimized metallization masks to reduce parasitic elements, smaller gate geometries, ion implanted ohmic contacts, an ion implanted

p^+-region beneath the gate, the characterization of a reliable p^+-GaAs epitaxial layer etchant, and others.

3. Try applying some of the MODFET I-V models reported in the literature to the (ESP)MODFET. Note however, that the DC models typically use fitting parameters (or allow changes to intrinsic resistances in circuit models) in order to match the theory to the measured results.

4. Theoretically analyze the various thermionic and tunneling emission mechanisms of the (ESP)MODFET and related structures, that lead to increased device noise. A starting point would be the standard equation for a metal/GaAs Schottky-barrier diode.

5. Fabricate MODFETs with varying strained channel thicknesses, substrate types, and epitaxial layer mole fractions, to deduce strain related effects on the MODFET's performance.

Appendix A

Charge-Control Model for an InGaAs/$Al_xGa_{1-x}As$ Enhanced Schottky-Barrier Pseudomorphic MODFET

Introduction

The first step in modelling the behavior of a MODFET is to obtain a solution to the one dimensional problem of charge control by an electrical gate [25:781]. In the first case of interest, the structure to be analyzed (Fig. A.1) consists of a Schottky-barrier contact placed upon a thin p^+-doped GaAs layer (Region IV) placed in turn on a thin layer of linearly graded n-doped $Al_xGa_{1-x}As$ (Region III). This is followed by an n-doped $Al_{0.15}Ga_{0.85}As$ layer (Region II) on an undoped $Al_{0.15}Ga_{0.85}As$ (about 30 Å) separation layer (Region I) on an unintentionally-doped $In_{0.15}Ga_{0.85}As$ (about 200 Å) channel layer. The channel layer has a background acceptor concentration (N_{AIn}) of about 1×10^{14} cm^{-3} and contains the quantized two-dimensional electron gas (2DEG) or transferred charge density n_s (units of cm^{-2}). The $In_{0.15}Ga_{0.85}As$ channel layer rests on a semi-insulating (S.I.) GaAs buffer layer (1μm thick again with $N_A \approx 1 \times 10^{14}$ cm^{-3}). The buffer layer is in turn grown on a S.I. GaAs substrate.

Each region of the MODFET structure is characterized by a permittivity ε (F/cm), doping density N_D (donor) or N_A (acceptor) (cm^{-3}), and thickness (Å). Several assumptions are made to simplify the mathematical charge-control derivation and are now presented:

1) All available donors and acceptors in the semiconductor layers are ionized in the depletion region;

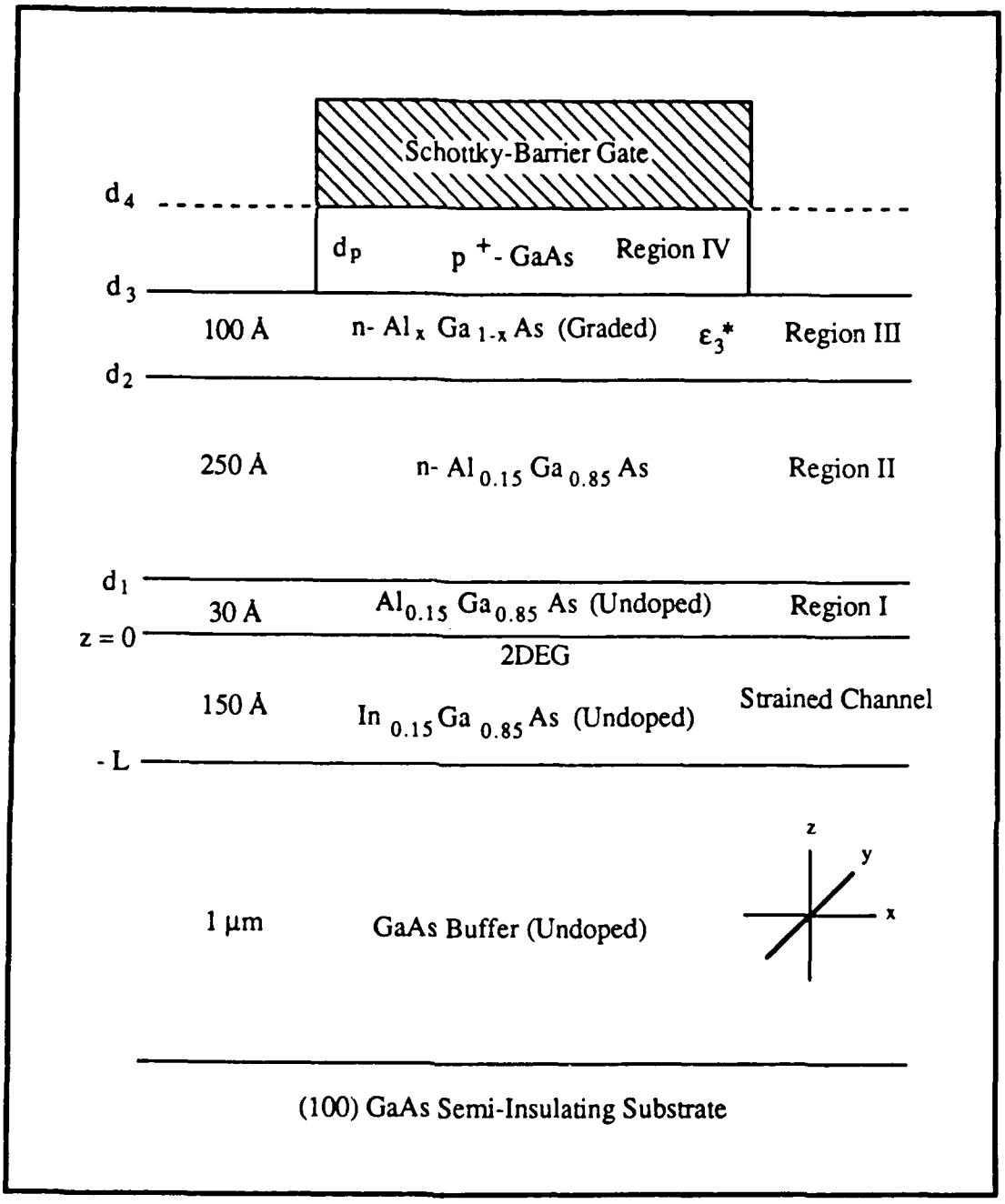


Fig. A.1 (ESP)MODFET Structure Used to Derive Charge-Control Model 1

2) The depletion approximation is valid, i.e., the mobile-carrier densities are negligible in the depletion region;

3) The electric field in the quantum well (E_o) is quasi-constant and equal to $- qn_s/\varepsilon_{In}$ [25:777];

4) The potential at the undoped heterojunction (V_o) is equal to $\Delta E_c - \Delta E_{F1}$, where ΔE_c is the conduction band energy discontinuity at the hetero-interface, and ΔE_{F1} is the energy difference between the Fermi energy level and the bottom of the quantum potential well at the hetero-interface;

5) The band discontinuities are independent of the doping densities;

6) The permittivity of $Al_xGa_{1-x}As$ (ε_3) is equal to $(13.18 - 3.12x)\varepsilon_o$ [1:R18];

7) The permittivity of $Al_xGa_{1-x}As$ in Regions I and II is assumed to be independent of doping density (e.g., $\varepsilon_1 = \varepsilon_2$);

8) The compositional grading of AlAs (e.g. the $Al_xGa_{1-x}As$ bandgap) is linear in Region III and may be described by an effective permittivity ε_3*;

9) The pseudomorphic approximation is valid for the structures of this study;

10) Each device region contains a uniform crystalline structure and homogeneous doping density (if doped);

11) The electric field perpendicular to the hetero-interface (z-direction) is much larger than the electric field parallel to the 2DEG between source and drain contacts.

An analytic expression relating the 2DEG density (n_s) to the applied gate potential (V_G) is achieved by using one final approximation in addition to the assumptions above. For $n_s > 5 \times 10^{11}$ cm $^{-2}$, the Fermi level (ΔE_{F1}) in the quasi-triangular quantum well of a normal MODFET may be taken as a linear function of n_s [25:776-782]. Thus

$$q\Delta E_{F1} = q\Delta E_{F0} + qan_s \qquad (eV) \qquad (2.2)$$

where a is equal to 0.125 x 10^{-12} volts-cm^2 and ΔE_{F0} is equal to zero at 300 °K [28]. The relationship between ΔE_{F1} and n_s in the InGaAs/AlGaAs MODFET (quasi-rectangular quantum well) will be approximated by (2.2).

Ideally, all the current in a MODFET is carried by the 2DEG. Thus the AlGaAs layers (and p^+-GaAs layer) must be entirely depleted of free carriers. Some fraction of the AlGaAs layers are depleted by charge transfer across the InGaAs/AlGaAs heterojunction while the rest are depleted by the Schottky-barrier gate potential (ϕ_B) and applied gate potential (V_G) (and the p^+-GaAs layer if used). Thus for a depletion mode device, the thicknesses of the AlGaAs layers are adjusted for total depletion without appreciably depleting any of the 2DEG. Alternately, the AlGaAs layer widths are reduced further and a gate bias must be applied to create the 2DEG (enhancement mode device).

Charge-Control Derivation

The charge-control model derivation for the MODFET of Fig. A.1 proceeds as follows. The electric field (E) and electrostatic potential (V) for each region of the MODFET is determined by solving Poisson's equation in each region, combined with appropriate boundary conditions. The boundary conditions are the continuity of electrical displacement (e.g., $\varepsilon_1 E_1(d_1) = \varepsilon_2 E_2(d_1)$ at the Region I-II boundary) and the continuity of electrostatic potential except for the discontinuities at heterojunctions (e.g. - $V_3(d_3)$ - ΔE_{c34} = - $V_4(d_3)$ where ΔE_{c34} is the conduction band potential energy difference between $Al_xGa_{1-x}As$ and GaAs at d_3). A convenient reference point ($z = 0$) is taken at the InGaAs/AlGaAs heterojunction as shown in Fig. A.1.

Electric Field

Region I ($0 \leq z \leq d_1$). The boundary condition in Region I at $z = 0$ is

$$\varepsilon_{In} E_o(0) = \varepsilon_1 E_1(0) \tag{A.1}$$

Using the assumption [21:956; 25:777] that the electric field is quasi-constant in the 2DEG:

$$E_o = - \frac{qn_s}{\varepsilon_{In}} \tag{A.2}$$

Substituting (A.2) into (A.1) and rearranging yields

$$\varepsilon_1 E_1(0) = - qn_s \tag{A.3}$$

The electric field in Region I (E_1) is found by integrating Poisson's equation, thus

$$- \frac{\partial^2 V_1}{\partial z^2} = \frac{\partial E_1}{\partial z} = \frac{\rho_1}{\varepsilon_1} = - \frac{q(n-p)}{\varepsilon_1} \tag{A.4}$$

$$\int \partial E_1(z) = E_1(z) = \int \frac{\rho_1}{\varepsilon_1} dz = \frac{\rho_1 z}{\varepsilon_1} + C_1 \tag{A.5}$$

where C_1 is a constant of integration. But since the $Al_{0.15}Ga_{0.85}As$ is undoped in Region I, ρ_1 is approximately equal to zero (neglecting image forces), and thus, (A.5) becomes

$$E_1(z) = C_1 \tag{A.6}$$

By substituting (A.3) into (A.6) at $z = 0$, an expression for the electric field in Region I can be found. Thus

$$E_1(0) = -\frac{qn_s}{\varepsilon_1} = C_1 \tag{A.7}$$

Substituting C_1 from (A.7) into (A.6) results in the final expression for the electric field in Region I:

$$E_1(z) = -\frac{qn_s}{\varepsilon_1} \quad (0 \le z \le d_1) \qquad \text{(volt/cm)} \tag{A.8}$$

Region II $(d_1 \le z \le d_2)$. The boundary condition in Region II at $z = d_1$ is

$$\varepsilon_1 E_1(d_1) = \varepsilon_2 E_2(d_1) \tag{A.9}$$

The electric field in Region II (E_2) is found by integrating Poisson's equation and assuming that ρ_2 is dominated by N_D, thus

$$-\frac{\partial^2 V_2}{\partial z^2} = \frac{\partial E_2}{\partial z} = \frac{\rho_2}{\varepsilon_2} = \frac{qN_D}{\varepsilon_2} \tag{A.10}$$

$$\int \partial E_2(z) = E_2(z) = \int \frac{\rho_2}{\varepsilon_2} dz = \int \frac{qN_D}{\varepsilon_2} dz = \frac{qN_D z}{\varepsilon_2} + C_2 \tag{A.11}$$

where C_2 is a constant of integration. By applying the boundary condition at $z = d_1$ (e.g. combining (A.8), (A.9), and (A.11)) and solving for C_2, an expression for the electric field in Region II can be found. Thus

$$\varepsilon_1\left(-\frac{qn_s}{\varepsilon_1}\right) = \varepsilon_2\left(\frac{qN_D d_1}{\varepsilon_2} + C_2\right) \tag{A.12}$$

$$C_2 = -\frac{qn_s}{\varepsilon_2} - \frac{qN_D d_1}{\varepsilon_2} \tag{A.13}$$

Substituting C_2 from (A.13) into (A.11) results in the final expression for the electric field in Region II:

$$E_2(z) = \frac{qN_D z}{\varepsilon_2} - \frac{qn_s}{\varepsilon_2} - \frac{qN_D d_1}{\varepsilon_2} \tag{A.14}$$

$$E_2(z) = -\frac{qn_s}{\varepsilon_2} - \frac{qN_D(d_1 - z)}{\varepsilon_2} \quad (d_1 \le z \le d_2) \quad \text{(volt/cm)} \tag{A.15}$$

Region III $(d_2 \le z \le d_3)$. The boundary condition in Region III at $z = d_2$ is

$$\varepsilon_2 E_2(d_2) = \varepsilon_3^* E_3(d_2) \tag{A.16}$$

The electric field in Region III (E_3) is found by integrating Poisson's equation and assuming that ρ_3 is dominated by N_D. By assuming an effective permittivity (ε_3^*) in Region III (see Appendix B for the case of a linear $\varepsilon_3(z)$), Poisson's equation may be written as follows:

$$-\frac{\partial^2 V_3}{\partial z^2} = \frac{\partial E_3}{\partial z} = \frac{\rho_3}{\varepsilon_3^*} = \frac{qN_D}{\varepsilon_3^*} \tag{A.17}$$

$$\int \partial E_3(z) = E_3(z) = \int \frac{\rho_3}{\varepsilon_3^*} dz = \int \frac{qN_D}{\varepsilon_3^*} dz = \frac{qN_D z}{\varepsilon_3^*} + C_3 \tag{A.18}$$

where C_3 is a constant of integration. By applying the boundary condition at $z = d_2$ (e.g. combining (A.15), (A.16), and (A.18)) and solving for C_3, an expression for the electric field in Region III can be found. Thus

$$-\varepsilon_2\left[\frac{qn_s}{\varepsilon_2}+\frac{qN_D(d_1-d_2)}{\varepsilon_2}\right]=\varepsilon_3^*\left[\frac{qN_Dd_2}{\varepsilon_3^*}+C_3\right] \tag{A.19}$$

$$C_3=-\frac{qn_s}{\varepsilon_3^*}-\frac{qN_D(d_1-d_2)}{\varepsilon_3^*}-\frac{qN_Dd_2}{\varepsilon_3^*} \tag{A.20}$$

$$C_3=-\frac{qn_s}{\varepsilon_3^*}-\frac{qN_Dd_1}{\varepsilon_3^*} \tag{A.21}$$

Substituting C_3 from (A.21) into (A.18) results in the final expression for the electric field in Region III:

$$E_3(z)=\frac{qN_Dz}{\varepsilon_3^*}-\frac{qn_s}{\varepsilon_3^*}-\frac{qN_Dd_1}{\varepsilon_3^*} \tag{A.22}$$

$$E_3(z)=-\frac{qn_s}{\varepsilon_3^*}-\frac{qN_D(d_1-z)}{\varepsilon_3^*} \quad (d_2 \le z \le d_3) \quad \text{(volt/cm)} \tag{A.23}$$

Region IV $(d_3 \le z \le d_4)$ The boundary condition in Region IV at $z = d_3$ is

$$\varepsilon_3^*E_3(d_3)=\varepsilon_4E_4(d_3) \tag{A.24}$$

The electric field in Region IV (E_4) is found by integrating Poisson's equation and assuming that ρ_4 is dominated by N_A, thus

$$-\frac{\partial^2 V_4}{\partial z^2} = \frac{\partial E_4}{\partial z} = \frac{\rho_4}{\varepsilon_4} = -\frac{qN_A}{\varepsilon_4} \tag{A.25}$$

$$\int \partial E_4(z) = E_4(z) = \int \frac{\rho_4}{\varepsilon_4} dz = \int -\frac{qN_A}{\varepsilon_4} dz = -\frac{qN_A z}{\varepsilon_4} + C_4 \tag{A.26}$$

where C_4 is a constant of integration. By applying the boundary condition at $z = d_3$ (e.g. combining (A.23), (A.24), and (A.26)) and solving for C_4, an expression for the electric field in Region IV can be found. Thus

$$\varepsilon_3^* \left[-\frac{qn_s}{\varepsilon_3^*} - \frac{qN_D(d_1 - d_3)}{\varepsilon_3^*} \right] = \varepsilon_4 \left[-\frac{qN_A d_3}{\varepsilon_4} + C_4 \right] \tag{A.27}$$

$$\varepsilon_4 C_4 = -qn_s - qN_D(d_1 - d_3) + qN_A d_3 \tag{A.28}$$

$$C_4 = -\frac{qn_s}{\varepsilon_4} - \frac{qN_D(d_1 - d_3)}{\varepsilon_4} + \frac{qN_A d_3}{\varepsilon_4} \tag{A.29}$$

Substituting C_4 from (A.29) into (A.26) results in the final expression for the electric field in Region IV:

$$E_4(z) = -\frac{qN_A z}{\varepsilon_4} - \frac{qn_s}{\varepsilon_4} - \frac{qN_D(d_1 - d_3)}{\varepsilon_4} + \frac{qN_A d_3}{\varepsilon_4} \tag{A.30}$$

$$E_4(z) = -\frac{qn_s}{\varepsilon_4} - \frac{qN_D(d_1 - d_3)}{\varepsilon_4} - \frac{qN_A(z - d_3)}{\varepsilon_4} \quad (d_3 \le z \le d_4) \quad \text{(volt/cm)} \tag{A.31}$$

The electric field vs. gate distance for the MODFET structure of Fig. A.1 can now be determined by using (A.8), (A.15), (A.23), and (A.31), given an initial value for n_s.

Electrostatic Potential

The electrostatic potential (V) for each region of the (ESP)MODFET is found by integrating the electric field in each region using Poisson's equation:

$$-\frac{\partial^2 V}{\partial z^2} = \frac{\partial E}{\partial z} = \frac{\rho}{\varepsilon} \tag{A.32}$$

$$-\int \partial V(z) = \int E(z)dz = -V(z) \tag{A.33}$$

The electrostatic potential equations will be used to construct an energy band diagram between the metal Schottky-barrier gate and the 2DEG channel of the MODFET.

Region I $(0 \leq z \leq d_1)$. The boundary condition in Region I at $z = 0$ is

$$-V_1(0) = \Delta E_c - \Delta E_{F1} \tag{A.34}$$

The electrostatic potential in Region I (V_1) is found by integrating the electric field in Region I (A.8) using Poisson's equation, thus

$$-\int \partial V_1(z) = \int E_1(z)dz = -V_1(z) = -\int \frac{qn_s}{\varepsilon_1}dz = -\frac{qn_s z}{\varepsilon_1} + C_5 \tag{A.35}$$

where C_5 is a constant of integration. By applying the boundary condition at $z = 0$ (e.g. combining (A.34) and (A.35)) and solving for C_5, an expression for the electrostatic potential in Region I is found as follows:

$$- V_1(0) = C_5 = \Delta E_c - \Delta E_{F1} \tag{A.36}$$

Substituting C_5 from (A.36) into (A.35) results in the final expression for the electrostatic potential in Region I:

$$- V_1(z) = \left(- \frac{qn_s z}{\varepsilon_1} + \Delta E_c - \Delta E_{F1} \right) \quad (0 \le z \le d_1) \quad \text{(volts)} \tag{A.37}$$

Region II $(d_1 \le z \le d_2)$. The boundary condition in Region II at $z = d_1$ is

$$- V_1(d_1) = - V_2(d_1) \tag{A.38}$$

The electrostatic potential in Region II (V_2) is found by integrating the electric field in Region *II* (A.15) using Poisson's equation, thus

$$- \int \partial V_2(z) = \int E_2(z) dz = - V_2(z) = - \int \left[\frac{qn_s}{\varepsilon_2} + \frac{qN_D(d_1 - z)}{\varepsilon_2} \right] dz \tag{A.39}$$

$$- V_2(z) = - \frac{qn_s z}{\varepsilon_2} - \frac{qN_D(2d_1 z - z^2)}{2\varepsilon_2} + C_6 \tag{A.40}$$

where C_6 is a constant of integration. By applying the boundary condition at $z = d_1$ (e.g. combining (A.37), (A.38), and (A.40)) and solving for C_6, an expression for the electrostatic potential in Region II is found as follows:

$$- \frac{qn_s d_1}{\varepsilon_1} + \Delta E_c - \Delta E_{F1} = - \frac{qn_s d_1}{\varepsilon_2} - \frac{qN_D(2d_1^2 - d_1^2)}{2\varepsilon_2} + C_6 \tag{A.41}$$

$$C_6 = \frac{qN_D d_1^2}{2\varepsilon_2} + \Delta E_c - \Delta E_{F1} \tag{A.42}$$

where the permittivity of $Al_xGa_{1-x}As$ in Regions I and II is assumed to be independent of doping density (e.g. $\varepsilon_1 = \varepsilon_2$). Substituting C_6 from (A.42) into (A.40) results in the final expression for the electrostatic potential in Region II:

$$-V_2(z) = -\frac{qn_s z}{\varepsilon_2} - \frac{qN_D(2d_1 z - z^2)}{2\varepsilon_2} + \frac{qN_D d_1^2}{2\varepsilon_2} + \Delta E_c - \Delta E_{F1} \tag{A.43}$$

$$-V_2(z) = -\frac{qn_s z}{\varepsilon_2} + \frac{qN_D(z - d_1)^2}{2\varepsilon_2} + \Delta E_c - \Delta E_{F1} \quad (d_1 \le z \le d_2) \quad \text{(volts)} \tag{A.44}$$

Region III ($d_2 \le z \le d_3$). The boundary condition in Region III at $z = d_2$ is

$$-V_2(d_2) = -V_3(d_2) \tag{A.45}$$

The electrostatic potential in Region III (V_3) is found by integrating the electric field in Region III (A.23) using Poisson's equation, thus

$$-\int \partial V_3(z) = \int E_3(z) = -V_3(z) = -\int \left[\frac{qn_s}{\varepsilon_3^*} + \frac{qN_D(d_1 - z)}{\varepsilon_3^*}\right] dz \tag{A.46}$$

$$-V_3(z) = -\frac{qn_s z}{\varepsilon_3^*} - \frac{qN_D(2d_1 z - z^2)}{2\varepsilon_3^*} + C_7 \tag{A.47}$$

where C_7 is a constant of integration. By applying the boundary condition at $z = d_2$ (e.g. combining (A.44), (A.45), and (A.47)) and solving for C_7, an expression for the electrostatic potential in Region III is found as follows:

$$-\frac{qn_s d_2}{\varepsilon_2}+\frac{qN_D(d_2-d_1)^2}{2\varepsilon_2}+\Delta E_c-\Delta E_{F1}=-\frac{qn_s d_2}{\varepsilon_3^*}-\frac{qN_D(2d_1d_2-d_2^2)}{2\varepsilon_3^*}+C_7 \qquad (A.48)$$

$$C_7=-\frac{qn_s}{\varepsilon_2}\left(d_2-\frac{d_2\varepsilon_2}{\varepsilon_3^*}\right)+\frac{qN_D}{2\varepsilon_2}\left[(d_2-d_1)^2+\frac{2d_1d_2\varepsilon_2}{\varepsilon_3^*}-\frac{d_2^2\varepsilon_2}{\varepsilon_3^*}\right]+\Delta E_c-\Delta E_{F1} \qquad (A.49)$$

Substituting C_7 from (A.49) into (A.47) results in the final expression for the electrostatic potential in Region III:

$$-V_3(z)=-\frac{qn_s z}{\varepsilon_3^*}-\frac{qN_D(2d_1z-z^2)}{2\varepsilon_3^*}-\frac{qn_s}{\varepsilon_2}\left(d_2-\frac{d_2\varepsilon_2}{\varepsilon_3^*}\right)+\frac{qN_D}{2\varepsilon_2}\left[(d_2-d_1)^2+\frac{2d_1d_2\varepsilon_2}{\varepsilon_3^*}-\frac{d_2^2\varepsilon_2}{\varepsilon_3^*}\right]+\Delta E_c-\Delta E_{F1} \qquad (A.50)$$

$$-V_3(z)=-\frac{qn_s}{\varepsilon_2}\left[\frac{z\varepsilon_2}{\varepsilon_3^*}+d_2-\frac{d_2\varepsilon_2}{\varepsilon_3^*}\right]+\frac{qN_D}{2\varepsilon_3^*}\left[z^2-2d_1z+\frac{(d_2-d_1)^2\varepsilon_3^*}{\varepsilon_2}+2d_1d_2-d_2^2\right]+\Delta E_c-\Delta E_{F1} \quad (d_2\le z\le d_3) \qquad (A.51)$$

(volts)

Region IV ($d_3 \le z \le d_4$). The boundary condition in Region IV at $z = d_3$ is

$$-V_3(d_3)-\Delta E_{c34}=-V_4(d_3) \qquad (A.52)$$

where ΔE_{c34} is the conduction band discontinuity at the Region III/IV heterointerface. The electrostatic potential in Region IV (V_4) is found by integrating the electric field in Region IV (A.23) using Poisson's equation, thus

$$-\int \partial V_4(z) = \int E_4(z)dz = -V_4(z) =$$

$$-\int \left[\frac{qn_s}{\varepsilon_4} + \frac{qN_D(d_1 - d_3)}{\varepsilon_4} + \frac{qN_A(z - d_3)}{\varepsilon_4} \right] dz \qquad (A.53)$$

$$-V_4(z) = -\frac{qn_s z}{\varepsilon_4} - \frac{qN_D(d_1 - d_3)z}{\varepsilon_4} - \frac{qN_A(z^2 - 2d_3 z)}{2\varepsilon_4} + C_8 \qquad (A.54)$$

where C_8 is a constant of integration. By applying the boundary condition at $z = d_3$ (e.g. combining (A.51), (A.52), and (A.54)) and solving for C_8, an expression for the electrostatic potential in Region IV is found as follows:

$$-\frac{qn_s}{\varepsilon_2}\left[\frac{d_3\varepsilon_2}{\varepsilon_3^*} + d_2 - \frac{d_2\varepsilon_2}{\varepsilon_3^*} \right] + \frac{qN_D}{2\varepsilon_3^*}\left[d_3^2 - 2d_1d_3 + \frac{(d_2 - d_1)^2\varepsilon_3^*}{\varepsilon_2} + 2d_1d_2 - d_2^2 \right] \qquad (A.55)$$
$$+ \Delta E_c - \Delta E_{F1} - \Delta E_{c34} = -\frac{qn_s d_3}{\varepsilon_4} - \frac{qN_D(d_1d_3 - d_3^2)}{\varepsilon_4} - \frac{qN_A(d_3^2 - 2d_3^2)}{2\varepsilon_4} + C_8$$

$$C_8 = -\frac{qn_s}{\varepsilon_2}\left[\frac{d_3\varepsilon_2}{\varepsilon_3^*} + d_2 - \frac{d_2\varepsilon_2}{\varepsilon_3^*} - \frac{d_3\varepsilon_2}{\varepsilon_4} \right] + \frac{qN_D}{2\varepsilon_3^*}\left[d_3^2 - 2d_1d_3 + \frac{(d_2 - d_1)^2\varepsilon_3^*}{\varepsilon_2} \right. \qquad (A.56)$$
$$\left. + 2d_1d_2 - d_2^2 + \frac{2d_1d_3\varepsilon_3^*}{\varepsilon_4} - \frac{2d_3^2\varepsilon_3^*}{\varepsilon_4} \right] - \frac{qN_Ad_3^2}{2\varepsilon_4} + \Delta E_c - \Delta E_{F1} - \Delta E_{c34}$$

Substituting C_8 from (A.56) into (A.54) results in the final expression for the electrostatic potential in Region IV:

$$-V_4(z) = -\frac{qn_s z}{\varepsilon_4} - \frac{qn_s}{\varepsilon_2}\left[\frac{d_3\varepsilon_2}{\varepsilon_3^*} + d_2 - \frac{d_2\varepsilon_2}{\varepsilon_3^*} - \frac{d_3\varepsilon_2}{\varepsilon_4}\right] - \frac{qN_D(d_1 - d_3)z}{\varepsilon_4}$$
$$+ \frac{qN_D}{2\varepsilon_3^*}\left[d_3^2 - 2d_1d_3 + \frac{(d_2 - d_1)^2\varepsilon_3^*}{\varepsilon_2} + 2d_1d_2 - d_2^2 + \frac{2d_1d_3\varepsilon_3^*}{\varepsilon_4} - \frac{2d_3^2\varepsilon_3^*}{\varepsilon_4}\right] \qquad \text{(A.57)}$$
$$- \frac{qN_A(z^2 - 2d_3z)}{2\varepsilon_4} - \frac{qN_Ad_3^2}{2\varepsilon_4} + \Delta E_c - \Delta E_{F1} - \Delta E_{c34}$$

$$-V_4(z) = -\frac{qn_s}{\varepsilon_2}\left[\frac{z\varepsilon_2}{\varepsilon_4} + \frac{d_3\varepsilon_2}{\varepsilon_3^*} + d_2 - \frac{d_2\varepsilon_2}{\varepsilon_3^*} - \frac{d_3\varepsilon_2}{\varepsilon_4}\right] - \frac{qN_A(z - d_3)^2}{2\varepsilon_4}$$
$$+ \frac{qN_D}{2\varepsilon_3^*}\left[\frac{2z\varepsilon_3^*(d_3 - d_1)}{\varepsilon_4} + d_3^2 - 2d_1d_3 + \frac{(d_2 - d_1)^2\varepsilon_3^*}{\varepsilon_2} + 2d_1d_2\right. \qquad \text{(A.58)}$$
$$\left. - d_2^2 + \frac{2d_1d_3\varepsilon_3^*}{\varepsilon_4} - \frac{2d_3^2\varepsilon_3^*}{\varepsilon_4}\right] + \Delta E_c - \Delta E_{F1} - \Delta E_{c34} \qquad (d_3 \le z \le d_4)$$

(volts)

Charge-Control Equations

Enhanced Schottky-Barrier Pseudomorphic MODFET. A charge control equation is now derived by using (A.58) to relate the 2DEG density (n_s) to the Schottky-barrier potential (ϕ_B) and applied potential (V_G) at the metal gate. The electrostatic potential ($- V_4(d_4)$) at the metal/p^+-GaAs Schottky-barrier interface must be equal to the Schottky-barrier gate potential minus the applied gate potential. Equating the electrostatic potential at the gate to (A.58) at $z = d_4$ yields

$$\phi_B - V_G = - V_4(d_4) \qquad \text{(A.59)}$$

Rearranging (A.59) in terms of n_s and using (2.2) yields

$$n_s = \frac{\varepsilon_2}{q(d^* + \Delta d)}(V_G - V_{OFF}^*) \quad (cm^{-2}) \qquad V_G > V_{OFF}^*$$
$$= 0 \qquad\qquad\qquad\qquad (cm^{-2}) \qquad V_G \le V_{OFF}^* \tag{A.60}$$

where

$$d^* = \frac{d_4\varepsilon_2}{\varepsilon_4} + \frac{d_3\varepsilon_2}{\varepsilon_3^*} + d_2 - \frac{d_2\varepsilon_2}{\varepsilon_3^*} - \frac{d_3\varepsilon_2}{\varepsilon_4} \qquad (Å) \tag{A.61}$$

$$\Delta d = \frac{a\varepsilon_2}{q} \qquad (Å) \tag{A.62}$$

$$V_{OFF}^* = \phi_B + \frac{qN_A(d_4 - d_3)^2}{2\varepsilon_4} - \frac{qN_D}{2\varepsilon_3^*}\left[\frac{2d_4\varepsilon_3^*(d_3 - d_1)}{\varepsilon_4} + d_3^2 - 2d_1d_3\right.$$
$$\left. + \frac{(d_2 - d_1)^2\varepsilon_3^*}{\varepsilon_2} + 2d_1d_2 - d_2^2 + \frac{2d_1d_3\varepsilon_3^*}{\varepsilon_4} - \frac{2d_3^2\varepsilon_3^*}{\varepsilon_4}\right] - \Delta E_c + \Delta E_{F0} + \Delta Ec_{34} \tag{A.63}$$

(volts)

The final form for n_s (A.60) is similar to that of Drummond et al. [25] for the normal MODFET (see (2.4) in Chapter 2). Thus the standard charge control model can be used for the (ESP)MODFET structure of Fig. A.1 by replacing V_{OFF} with V_{OFF}^* and d with d*.

Pseudomorphic MODFET. For the case of the pseudomorphic MODFET (Fig. A.1 without a p^+-GaAs layer), the electrostatic potential at the metal/AlGaAs interface is solved as in (A.59) through (A.63). Equating the electrostatic potential at the gate to $-V_3(d_3)$ (e.g. setting $z = d_3$ in (A.51)) yields

$$\phi_B - V_G = - V_3(d_3) \tag{A.64}$$

Rearranging (A.64) in terms of n_s and using (2.2) yields

$$n_s = \frac{\varepsilon_2}{q\left(\frac{a\varepsilon_2}{q} + \frac{d_3\varepsilon_2}{\varepsilon_3^*} + d_2 - \frac{d_2\varepsilon_2}{\varepsilon_3^*}\right)}\left\{ V_G - \phi_B \right.$$

$$\left. + \frac{qN_D}{2\varepsilon_3^*}\left[d_3^2 - 2d_1d_3 + \frac{(d_2 - d_1)^2\varepsilon_3^*}{\varepsilon_2} + 2d_1d_2 - d_2^2 \right] + \Delta E_c - \Delta E_{F0} \right\} \quad V_G > V_{OFF}^* \tag{A.65}$$

$$= 0 \qquad V_G \le V_{OFF}^*$$

which also may be written in the form of (2.4).

Appendix B

Charge-Control Model for a Graded-Layer InGaAs/$Al_xGa_{1-x}As$ Enhanced Schottky-Barrier Pseudomorphic MODFET

Introduction

The MODFET structure to be analyzed is illustrated in Fig. B.1. The objective is to obtain a solution to the one-dimensional problem of charge control by an electrical gate. In other words, to relate the 2DEG density (n_s) to the applied gate voltage (V_G) and the built-in Schottky-barrier gate potential (ϕ_B), in addition to other physical parameters including: doping densities (N_D and N_A), permittivities (ε), and epitaxial layer thicknesses. The derivation proceeds in an analogous fashion as in Appendix A, except that Poisson's equation must be modified to account for the inhomogeneous nature of the material (since the permittivity in Region III is not constant but is assumed to vary with position $\varepsilon_3(z)$).

Several assumptions are made to simplify the mathematical charge-control derivation and are now presented:

1) All available donors and acceptors in the semiconductor layers are ionized in the depletion region;

2) The depletion approximation is valid, i.e., the mobile-carrier densities are negligible in the depletion region;

3) The electric field in the quantum well (E_o) is quasi-constant and equal to $-qn_s/\varepsilon_{In}$ [25:777];

4) The potential at the undoped heterojunction (V_o) is equal to $\Delta E_c - \Delta E_{F1}$, where ΔE_c is the conduction band energy discontinuity at the hetero-interface, and ΔE_{F1} is the

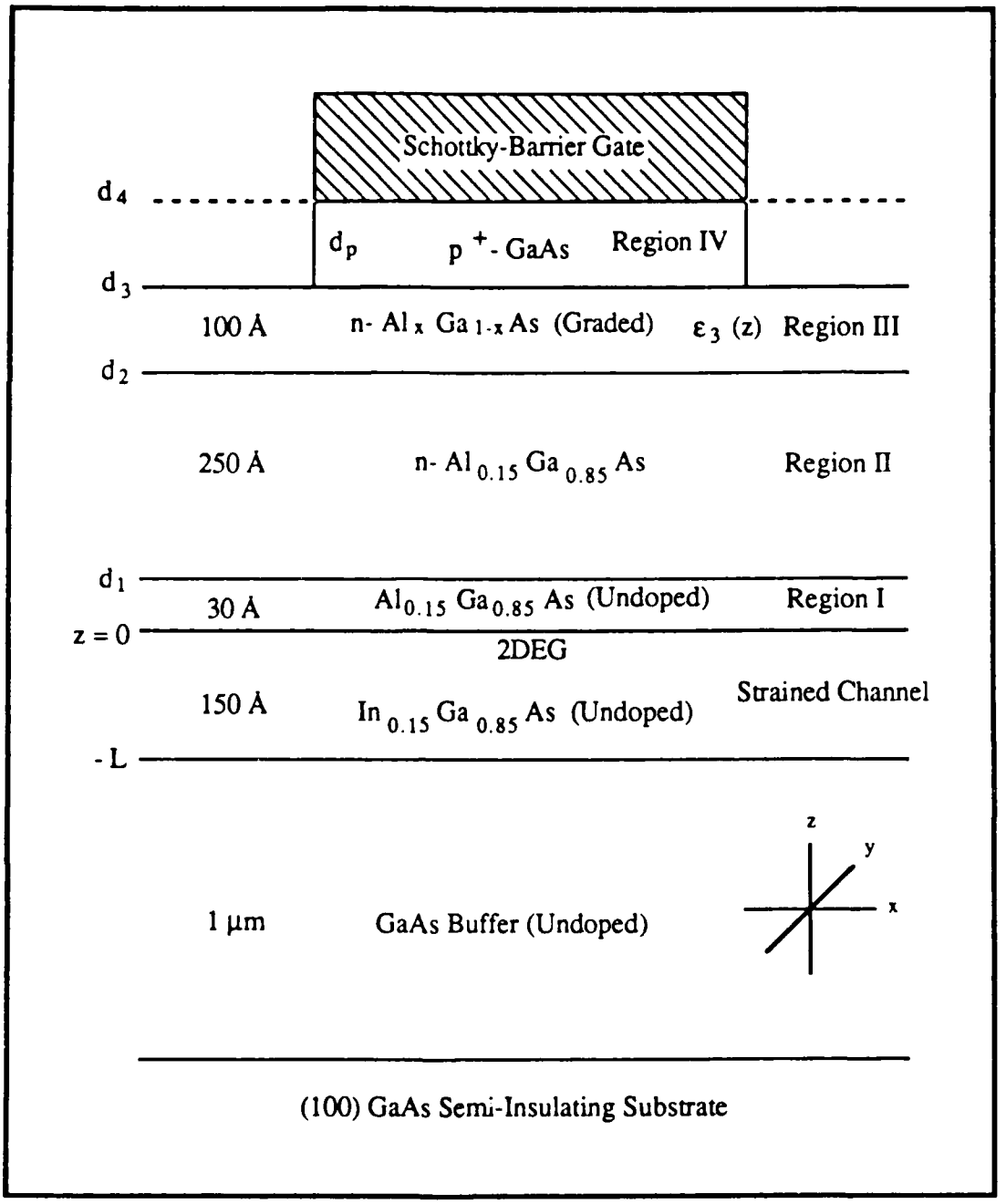


Fig. B.1 (ESP)MODFET Structure Used to Derive Charge-Control Model 2

energy difference between the Fermi energy level and the bottom of the quantum potential well at the hetero-interface;

5) The band discontinuities are independent of the doping densities;

6) The permittivity of $Al_xGa_{1-x}As$ (ε_3) is equal to $(13.18 - 3.12x)\varepsilon_o$ [1:R18];

7) The permittivity of $Al_xGa_{1-x}As$ in Regions I and II is assumed to be independent of doping density (e.g., $\varepsilon_1 = \varepsilon_2$);

8) The compositional grading of the AlAs mole fraction (e.g. the $Al_xGa_{1-x}As$ bandgap) is linear in Region III and the permittivity is given by $\varepsilon_3(z)$;

9) The pseudomorphic approximation is valid for the structures of this study;

10) Each device region contains a uniform crystalline structure and homogeneous doping density (if doped);

11) The electric field perpendicular to the heterointerface (z-direction) is much larger than the electric field parallel to the 2DEG between source and drain contacts.

An analytic expression relating the 2DEG density (n_s) to the applied gate potential (V_G) is achieved by using one final approximation in addition to the assumptions above. For $n_s > 5 \times 10^{11}$ cm $^{-2}$, the Fermi level position (ΔE_{F1}) in the quasi-triangular quantum well of a normal MODFET may be taken as a linear function of n_s [25:776-782]. Thus

$$q\Delta E_{F1} = q\Delta E_{F0} + qan_s \quad (eV) \tag{2.2}$$

where a is equal to 0.125×10^{-12} V-cm^2 and ΔE_{F0} is equal to zero at 300 °K [28]. The relationship between ΔE_{F1} and n_s in the InGaAs/AlGaAs MODFET (quasi-rectangular quantum well) will be approximated by (2.2).

Charge-Control Derivation

The charge-control model derivation for the MODFET of Fig. B.1 proceeds as follows. The electric field (E) and electrostatic potential (V) for each region of the MODFET is determined by solving Poisson's equation in each region, combined with appropriate boundary conditions. The boundary conditions are the continuity of electrical displacement (e.g. $\varepsilon_2 E_2(d_2) = \varepsilon_3(d_2)E_3(d_2)$ at the Region II-III boundary) and the continuity of electrostatic potential except for the discontinuities at heterojunctions (e.g., $-V_1(0) = \Delta E_c - \Delta E_{F1}$). A convenient reference point ($z = 0$) is taken at the InGaAs/AlGaAs (2DEG) heterojunction as shown in Fig. B.1.

For a heterojunction device with a relative permittivity ($\varepsilon_r(z)$) that varies according to the position and composition in the materials of the device, Poisson's equation must be modified to account for the inhomogeneous nature of the material [80:137]:

$$\nabla\cdot\{[\varepsilon_o\varepsilon_r(z)]E(z)\} = \rho(z) \tag{B.1}$$

Using the chain rule, (B.1) becomes

$$E(z)\cdot\nabla[\varepsilon_o\varepsilon_r(z)] + \varepsilon_o\varepsilon_r(z)\nabla\cdot E(z) = \rho(z) \tag{B.2}$$

For a one-dimensional analysis, (B.2) may be rewritten as

$$\frac{E(z)\partial[\varepsilon_o\varepsilon_r(z)]}{\partial z} + \varepsilon_o\varepsilon_r(z)\frac{\partial E(z)}{\partial z} = \rho(z) \tag{B.3}$$

$$\frac{\partial E(z)}{\partial z} = \frac{\rho(z)}{\varepsilon_o\varepsilon_r(z)} - \frac{E(z)}{\varepsilon_o\varepsilon_r(z)}\frac{\partial[\varepsilon_o\varepsilon_r(z)]}{\partial z} \tag{B.4}$$

Substituting for the electric field in terms of the electrostatic potential (e.g. $-\partial V/\partial z = E(z)$), (B.4) becomes

$$-\frac{\partial^2 V}{\partial z^2} = \frac{\rho(z)}{\varepsilon_o \varepsilon_r(z)} + \frac{\partial V}{\partial z}\frac{\partial[\varepsilon_o \varepsilon_r(z)]}{\partial z}\frac{1}{\varepsilon_o \varepsilon_r(z)} \qquad \text{(B.5)}$$

Electric Field

Region I and II $(0 \le z \le d_2)$. Equations for the electric field in Regions I and II were determined in Appendix A and are given by the following:

$$E_1(z) = -\frac{qn_s}{\varepsilon_1} \quad (0 \le z \le d_1) \qquad \text{(volt/cm)} \qquad \text{(A.8)}$$

$$E_2(z) = -\frac{qn_s}{\varepsilon_2} - \frac{qN_D(d_1 - z)}{\varepsilon_2} \quad (d_1 \le z \le d_2) \quad \text{(volt/cm)} \qquad \text{(A.15)}$$

Region III $(d_2 \le z \le d_3)$. A solution to (B.4) must be found in order to determine the electric field in Region III. Rewriting (B.4) by substituting for the charge density:

$$\frac{\partial E_3(z)}{\partial z} = \frac{q[N_D - n(z) + p(z) - N_A]}{\varepsilon_o \varepsilon_r(z)} - \frac{E_3(z)}{\varepsilon_o \varepsilon_r(z)}\frac{\partial[\varepsilon_o \varepsilon_r(z)]}{\partial z} \qquad \text{(B.6)}$$

The n-$Al_xGa_{1-x}As$ epitaxial layer is graded between $d_2 \le z \le d_3$. In other words, the AlAs mole fraction x(z) is a function of position as is the bandgap energy ($E_g(z)$) and the relative permittivity ($\varepsilon_r(z)$) of the n-$Al_xGa_{1-x}As$ epitaxial layer. The grading distribution function is controlled via the molecular-beam epitaxy (MBE) growth process. In general, the change of permittivity with distance (z) may be modelled as a power series in z as follows:

$$\varepsilon_o\varepsilon_r(z) = \varepsilon_o[C_0 + C_1 z + C_2 z^2 + \ldots + C_n z^n + \ldots] \tag{B.7}$$

where C_0, C_1, C_2, . . . are constants. Integration of (B.7) is straight-forward for substitution into (B.6). Alternately, a specific grading function may be attempted during MBE growth (within physical limitations) and then experimentally determined. Example grading functions include: exponential and hyperbolic tangential [11; 15]. A linear grading function will be assumed in this thesis.

The permittivity of $Al_xGa_{1-x}As$ (Region III) is given to first order by [1:R18]

$$\varepsilon_3(x) = (13.18 - 3.12x)\varepsilon_o = \varepsilon_o\varepsilon_{r3}(x) \tag{B.8}$$

where x is the AlAs mole fraction and ε_o is the permittivity of vacuum. A linear grading scheme is illustrated in Fig. B.2. An equation for the linear grading is simply that of a line:

$$x = Az + B \tag{B.9}$$

where A is the slope of the line and B is the ordinate (x) intercept. The slope of the line in Fig. B.2 is

$$A = \frac{x_2 - x_1}{d_3 - d_2} = \frac{\Delta x}{d_g} \tag{B.10}$$

where d_g is the thickness (Å) of the graded $Al_xGa_{1-x}As$ epitaxial layer. Substituting (B.10) into (B.9) and solving for B results in

$$B = x - \frac{\Delta x}{d_g} z \tag{B.11}$$

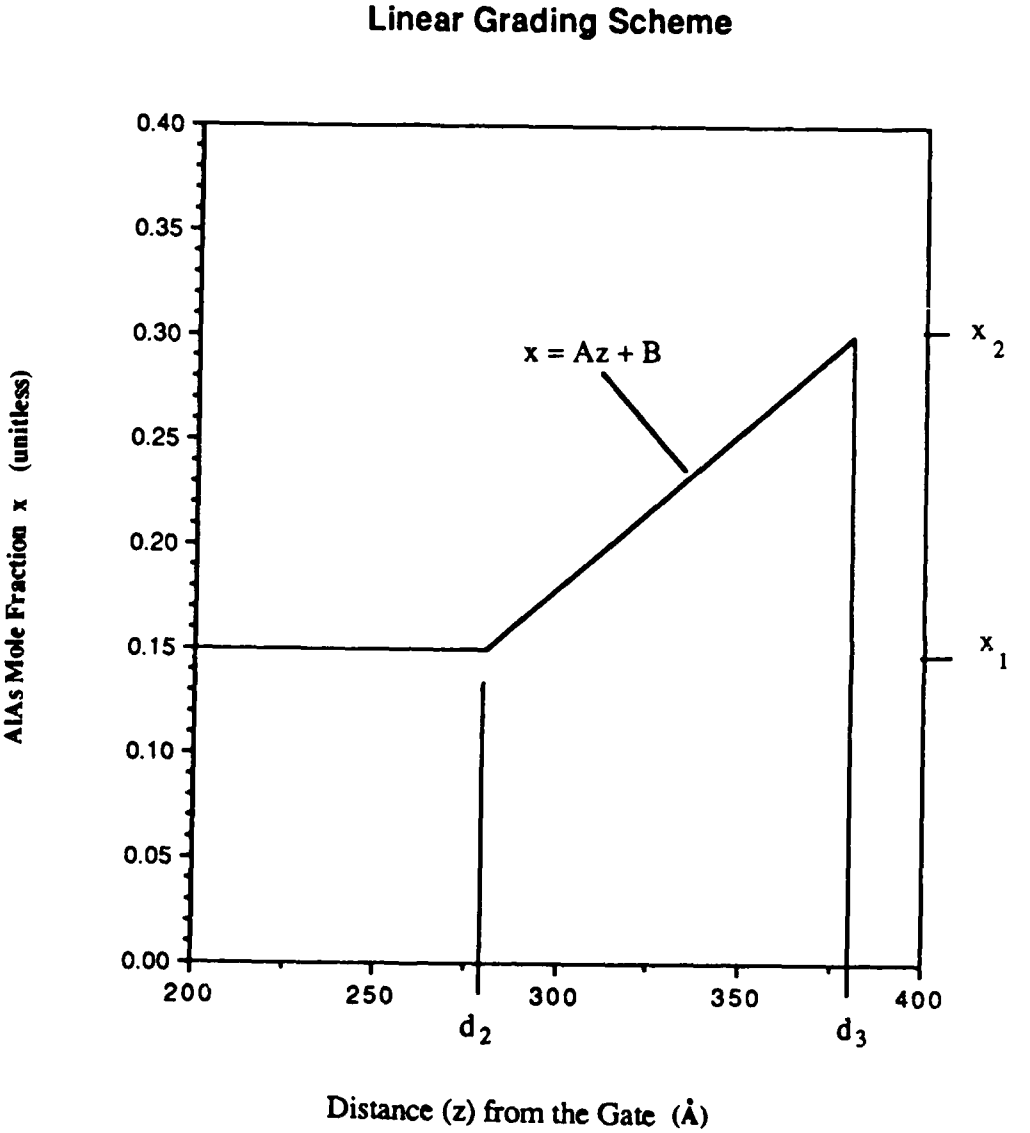


Fig. B.2 A Linear Grading Scheme

At $z = d_2$, $x = x_1$ and (B.11) becomes

$$B = x_1 - \frac{\Delta x}{d_g} d_2 \tag{B.12}$$

The final expression for the permittivity of a linearly graded $Al_xGa_{1-x}As$ epitaxial layer is found by substituting (B.10) and (B.12) into (B.9), and then (B.9) into (B.8) resulting in

$$\varepsilon_3(z) = \varepsilon_o \left\{ 13.18 - 3.12 \left[\frac{\Delta x}{d_g} z + \left(x_1 - \frac{\Delta x}{d_g} d_2 \right) \right] \right\} \tag{B.13}$$

Rearranging (B.13) and assigning constants (K_1 and K_2) gives

$$\varepsilon_3(z) = K_1 + K_2 z = \varepsilon_o \varepsilon_{r3}(z) \tag{B.14}$$

where

$$K_1 = \left[13.18 - 3.12 \left(x_1 - \frac{\Delta x}{d_g} d_2 \right) \right] \varepsilon_o \tag{B.15}$$

$$K_2 = - \left[3.12 \left(\frac{\Delta x}{d_g} \right) \right] \varepsilon_o \tag{B.16}$$

It is seen that (B.14) has the form of a power series (first two terms). From (B.14), the derivative of the permittivity in Region III is easily obtained as follows:

$$\frac{\partial \varepsilon_3(z)}{\partial z} = \frac{\partial (K_1 + K_2 z)}{\partial z} = K_2 \tag{B.17}$$

A solution that satisfies (B.6) will now be found in order to solve for the electric field in Region III. By assigning constants (K_2 from (B.16), and K_3), using (B.14) and (B.17), and rearranging, (B.6) becomes

$$\frac{\partial E_3(z)}{\partial z} + \frac{E_3(z)K_2}{\varepsilon_3(z)} = \frac{K_3}{\varepsilon_3(z)} \tag{B.18}$$

where

$$K_3 = \rho_3(z) = q(N_D - N_A - n(z) + p(z)) \approx qN_D \tag{B.19}$$

As shown, (B.18) is a first order linear differential equation and may be solved by using an integrating factor [99:74-76]. For an equation of the form

$$\frac{\partial y}{\partial z} + P(z)y = f(z) \tag{B.20}$$

where P(z) and f(z) are functions of z, the integrating factor (I.F.) is

$$\text{I.F.} = \exp\left[\int P(z)dz\right] \tag{B.21}$$

Multiplying each term of (B.20) by the I.F. results in

$$\frac{\partial y}{\partial z}\exp\left[\int P(z)dz\right] + P(z)y\exp\left[\int P(z)dz\right] = f(z)\exp\left[\int P(z)dz\right] \tag{B.22}$$

$$\frac{\partial}{\partial z}\left\{ y\exp\left[\int P(z)dz\right]\right\} = f(z)\exp\left[\int P(z)dz\right] \tag{B.23}$$

Integrating both sides of (B.23) results in a solution for y (which equals $E_3(z)$). For the present case, the integrating factor is

$$\text{I.F.} = \exp\left\{\int\left[\frac{K_2}{\varepsilon_3(z)}\right]dz\right\} = \exp\left\{\int\left[\frac{K_2}{K_1 + K_2 z}\right]dz\right\} \tag{B.24}$$

where $\varepsilon_3(z) = K_1 + K_2 z$ is given by (B.14). The integral in (B.24) is solved as follows: let

$$u = K_1 + K_2 z \tag{B.25}$$

then

$$dz = \frac{du}{K_2} \tag{B.26}$$

Substituting (B.25) and (B.26) into (B.24) gives

$$\text{I.F.} = \exp\left[K_2 \int\left(\frac{du}{K_2 u}\right)\right] = \exp\left(\int \frac{du}{u}\right) = \exp(\ln u) = u \tag{B.27}$$

Thus the integrating factor is simply u from (B.25). Multiplying each term of (B.18) by the integrating factor (as in (B.23)) and then integrating both sides yields

$$\frac{u\partial E_3(z)}{\partial z} + \frac{uE_3(z)K_2}{u} = \frac{\partial[uE_3(z)]}{\partial z} = \frac{uK_3}{u} \tag{B.28}$$

$$\int \partial[uE_3(z)] = \int K_3 \partial z = uE_3(z) = K_3 z + C_3 \tag{B.29}$$

where C_3 is a constant of integration. Substituting (B.14) and (B.19) into (B.29) and rearranging yields

$$E_3(z) = \frac{\rho_3 z}{\varepsilon_3(z)} + \frac{C_3}{\varepsilon_3(z)} \tag{B.30}$$

It is assumed that (B.30) is a solution to (B.6) for the case of a linearly varying permittivity. To verify the solution, $E_3(z)$ from (B.30) may be substituted into (B.3).

The electric field in Region III may now be found. The boundary condition in Region III at $z = d_2$ is

$$\varepsilon_2 E_2(d_2) = \varepsilon_3(d_2) E_3(d_2) \tag{B.31}$$

By applying the boundary condition at $z = d_2$ (e.g. combining (A.15), (B.30), and (B.31)) and solving for C_3, an expression for the electric field in Region III can be found:

$$\varepsilon_2\left[-\frac{qn_s}{\varepsilon_2} - \frac{qN_D(d_1 - d_2)}{\varepsilon_2}\right] = \varepsilon_3(d_2)\left[\frac{qN_D d_2}{\varepsilon_3(d_2)} + \frac{C_3}{\varepsilon_3(d_2)}\right] \tag{B.32}$$

$$C_3 = -qn_s - qN_D d_1 \tag{B.33}$$

Substituting C_3 from (B.33) into (B.30) results in the final expression for the electric field in Region III:

$$E_3(z) = \frac{qN_D z}{\varepsilon_3(z)} - \frac{qn_s}{\varepsilon_3(z)} - \frac{qN_D d_1}{\varepsilon_3(z)} \tag{B.34}$$

$$E_3(z) = -\frac{qn_s}{\varepsilon_3(z)} - \frac{qN_D(d_1 - z)}{\varepsilon_3(z)} \qquad (d_2 \le z \le d_3) \quad \text{(volt/cm)} \qquad \text{(B.35)}$$

Region IV $(d_3 \le z \le d_4)$ The boundary condition in Region IV at $z = d_3$ is

$$\varepsilon_3(d_3)E_3(d_3) = \varepsilon_4 E_4(d_3) \qquad \text{(B.36)}$$

The electric field in Region IV (E_4) is found by integrating Poisson's equation and assuming that ρ_4 is dominated by N_A, thus

$$-\frac{\partial^2 V_4}{\partial z^2} = \frac{\partial E_4(z)}{\partial z} = \frac{\rho_4}{\varepsilon_4} = -\frac{qN_A}{\varepsilon_4} \qquad \text{(B.37)}$$

$$\int \partial E_4(z) = E_4(z) = \int \frac{\rho_4}{\varepsilon_4} dz = -\int \frac{qN_A}{\varepsilon_4} dz = -\frac{qN_A z}{\varepsilon_4} + C_4 \qquad \text{(B.38)}$$

where C_4 is a constant of integration. By applying the boundary condition at $z = d_3$ (e.g. combining (B.35), (B.36), and (B.38)) and solving for C_4, an expression for the electric field in Region IV can be found. Thus

$$\varepsilon_3(d_3)\left[-\frac{qn_s}{\varepsilon_3(d_3)} - \frac{qN_D(d_1 - d_3)}{\varepsilon_3(d_3)}\right] = \varepsilon_4\left[-\frac{qN_A d_3}{\varepsilon_4} + C_4\right] \qquad \text{(B.39)}$$

$$\varepsilon_4 C_4 = -qn_s - qN_D(d_1 - d_3) + qN_A d_3 \qquad \text{(B.40)}$$

$$C_4 = -\frac{qn_s}{\varepsilon_4} - \frac{qN_D(d_1 - d_3)}{\varepsilon_4} + \frac{qN_A d_3}{\varepsilon_4} \qquad \text{(B.41)}$$

Substituting C_4 from (B.41) into (B.38) results in the final expression for the electric field in Region IV:

$$E_4(z) = -\frac{qN_A z}{\varepsilon_4} - \frac{qn_s}{\varepsilon_4} - \frac{qN_D(d_1 - d_3)}{\varepsilon_4} + \frac{qN_A d_3}{\varepsilon_4} \tag{B.42}$$

$$E_4(z) = -\frac{qn_s}{\varepsilon_4} - \frac{qN_D(d_1 - d_3)}{\varepsilon_4} - \frac{qN_A(z - d_3)}{\varepsilon_4} \quad (d_3 \le z \le d_4) \text{ (volt/cm)} \tag{B.43}$$

The electric field vs. gate distance for the MODFET structure of Fig. B.1 can now be determined by using (A.8), (A.15), (B.35), and (B.43), given an initial value for n_s.

Electrostatic Potential

The electrostatic potential (V) for each region of the MODFET structure of Fig. B.1 is found by integrating the electric field in each region using the relation:

$$-\frac{\partial^2 V}{\partial z^2} = \frac{\partial E}{\partial z} = \frac{\rho}{\varepsilon} \tag{B.44}$$

$$-\int \partial V(z) = \int E(z)dz = -V(z) \tag{B.45}$$

The electrostatic potential equations will be used to construct an energy band diagram between the metal gate and 2DEG channel of the MODFET structure of Fig. B.1.

Region I and II $(0 \le z \le d_2)$. Equations for the electrostatic potential in Regions I and II were determined in Appendix A and are given by the following:

$$-V_1(z) = \left(-\frac{qn_s z}{\varepsilon_1} + \Delta E_c - \Delta E_{F1}\right) \quad (0 \le z \le d_1) \quad \text{(volts)} \tag{A.37}$$

$$-V_2(z) = -\frac{qn_s z}{\varepsilon_2} + \frac{qN_D(z-d_1)^2}{2\varepsilon_2} + \Delta E_c - \Delta E_{F1} \quad (d_1 \le z \le d_2) \quad \text{(volts)} \tag{A.44}$$

Region III ($d_2 \le z \le d_3$). The boundary condition in Region III at $z = d_2$ is

$$-V_2(d_2) = -V_3(d_2) \tag{B.46}$$

The electrostatic potential in Region III ($V_3(z)$) is found by integrating the electric field in Region III (B.35) using Poisson's equation, thus

$$-V_3(z) = -\int\left[\frac{qn_s}{\varepsilon_3(z)} + \frac{qN_D(d_1-z)}{\varepsilon_3(z)}\right]dz \tag{B.47}$$

Substituting $\varepsilon_3(z) = K_1 + K_2 z$ from (B.14) into (B.47), the two integral terms of (B.47) may be solved as follows [9: 238]:

$$\int\left(\frac{qn_s}{K_1 + K_2 z}\right)dz = qn_s\int\frac{dz}{K_1 + K_2 z} = \frac{qn_s}{K_2}[\ln(K_1 + K_2 z)] + C \tag{B.48}$$

and

$$\int\left[\frac{qN_D(d_1-z)}{\varepsilon_3(z)}\right]dz =$$

$$\frac{qN_D d_1}{K_2}[\ln(K_1 + K_2 z)] - qN_D\left[\frac{z}{K_2} - \frac{K_1}{(K_2)^2}\ln(K_1 + K_2 z)\right] + C \tag{B.49}$$

where the C's are constants. By substituting (B.48) and (B.49) into (B.47) and combining constants, the electrostatic potential in Region III may be written

$$-V_3(z) = -\frac{qn_s}{K_2}[\ln(K_1 + K_2 z)] - \frac{qN_D d_1}{K_2}[\ln(K_1 + K_2 z)] + qN_D\left[\frac{z}{K_2} - \frac{K_1}{(K_2)^2}\ln(K_1 + K_2 z)\right] + C_7 \tag{B.50}$$

where C_7 is a constant of integration. By applying the boundary condition at $z = d_2$ (e.g. combining (A.44), (B.46), and (B.50)) and solving for C_7, an expression for the electrostatic potential in Region III is found as follows:

$$-\frac{qn_s d_2}{\varepsilon_2} + \frac{qN_D(d_2 - d_1)^2}{2\varepsilon_2} + \Delta E_c - \Delta E_{F1} = -\frac{qn_s}{K_2}[\ln(K_1 + K_2 d_2)] - qN_D\left[\frac{d_1}{K_2}\ln(K_1 + K_2 d_2) - \frac{d_2}{K_2} + \frac{K_1}{(K_2)^2}\ln(K_1 + K_2 d_2)\right] + C_7 \tag{B.51}$$

$$C_7 = -qn_s\left[\frac{d_2}{\varepsilon_2} - \frac{1}{K_2}\ln(K_1 + K_2 d_2)\right] + qN_D\left[\frac{(d_2 - d_1)^2}{2\varepsilon_2} + \frac{d_1}{K_2}\ln(K_1 + K_2 d_2) - \frac{d_2}{K_2} + \frac{K_1}{(K_2)^2}\ln(K_1 + K_2 d_2)\right] + \Delta E_c - \Delta E_{F1} \tag{B.52}$$

Substituting C_7 from (B.52) into (B.50) results in the final expression for the electrostatic potential in Region III:

$$-V_3(z) = -qn_s\left[\frac{1}{K_2}\ln(K_1 + K_2z) + \frac{d_2}{\varepsilon_2} - \frac{1}{K_2}\ln(K_1 + K_2d_2)\right]$$
$$+ qN_D\left[\frac{(d_2 - d_1)^2}{2\varepsilon_2} + \frac{d_1}{K_2}\ln(K_1 + K_2d_2) - \frac{d_1}{K_2}\ln(K_1 + K_2z) + \frac{z}{K_2} - \frac{d_2}{K_2}\right. \quad \text{(B.53)}$$
$$\left. + \frac{K_1}{(K_2)^2}\ln(K_1 + K_2d_2) - \frac{K_1}{(K_2)^2}\ln(K_1 + K_2z)\right] + \Delta E_c - \Delta E_{F1}$$

$$-V_3(z) = qn_s\left[\frac{1}{K_2}\ln\left(\frac{K_1 + K_2d_2}{K_1 + K_2z}\right) - \frac{d_2}{\varepsilon_2}\right] + \Delta E_c - \Delta E_{F1}$$
$$+ qN_D\left\{\frac{(d_2 - d_1)^2}{2\varepsilon_2} + \left[\frac{d_1}{K_2} + \frac{K_1}{(K_2)^2}\right]\left[\ln\left(\frac{K_1 + K_2d_2}{K_1 + K_2z}\right)\right] + \frac{(z - d_2)}{K_2}\right\} \quad (d_2 \le z \le d_3) \quad \text{(B.54)}$$

(volts)

Region IV ($d_3 \le z \le d_4$). The boundary condition in Region IV at $z = d_3$ is

$$-V_3(d_3) - \Delta E_{c34} = -V_4(d_3) \quad \text{(B.55)}$$

The electrostatic potential in Region IV (V_4) is found by integrating the electric field in Region IV (B.43) using Poisson's equation, thus

$$-\int \partial V_4(z) = -V_4(z) = \int E_4(z)dz =$$
$$-\int\left[\frac{qn_s}{\varepsilon_4} + \frac{qN_D(d_1 - d_3)}{\varepsilon_4} + \frac{qN_A(z - d_3)}{\varepsilon_4}\right]dz \quad \text{(B.56)}$$

$$-V_4(z) = -\frac{qn_sz}{\varepsilon_4} - \frac{qN_D(d_1 - d_3)z}{\varepsilon_4} - \frac{qN_A(z^2 - 2d_3z)}{2\varepsilon_4} + C_8 \quad \text{(B.57)}$$

where C_8 is a constant of integration. By applying the boundary condition at $z = d_3$ (e.g. combining (B.54), (B.55), and (B.57)) and solving for C_8, an expression for the electrostatic potential in Region IV is found as follows:

$$qn_s\left[\frac{1}{K_2}\ln(K_4) - \frac{d_2}{\varepsilon_2}\right] + qN_D\left\{\frac{(d_2-d_1)^2}{2\varepsilon_2} + \left[\frac{d_1}{K_2} + \frac{K_1}{(K_2)^2}\right][\ln(K_4)] + \frac{(d_3-d_2)}{K_2}\right\} \quad \text{(B.58)}$$

$$+ \Delta E_c - \Delta E_{F1} - \Delta E_{c34} = -\frac{qn_s d_3}{\varepsilon_4} - \frac{qN_D(d_1 d_3 - d_3^2)}{\varepsilon_4} - \frac{qN_A(d_3^2 - 2d_3^2)}{2\varepsilon_4} + C_8$$

where

$$K_4 = \frac{K_1 + K_2 d_2}{K_1 + K_2 d_3}$$

and thus the constant C_8 may be written

$$C_8 = qn_s\left[\frac{1}{K_2}\ln(K_4) - \frac{d_2}{\varepsilon_2} + \frac{d_3}{\varepsilon_4}\right] - \frac{qN_A d_3^2}{2\varepsilon_4} + \Delta E_c - \Delta E_{F1} - \Delta E_{c34}$$

$$+ qN_D\left\{\frac{(d_2-d_1)^2}{2\varepsilon_2} + \frac{(d_3-d_2)}{K_2} + \frac{(d_1 d_3 - d_3^2)}{\varepsilon_4} + \left[\frac{d_1}{K_2} + \frac{K_1}{(K_2)^2}\right][\ln(K_4)]\right\} \quad \text{(B.59)}$$

Substituting C_8 from (B.59) into (B.57) results in the final expression for the electrostatic potential in Region IV:

$$-V_4(z) = -\frac{qn_s z}{\varepsilon_4} - \frac{qN_D(d_1 - d_3)z}{\varepsilon_4} - \frac{qN_A(z^2 - 2d_3 z)}{2\varepsilon_4}$$

$$+ qn_s\left[\frac{1}{K_2}\ln(K_4) - \frac{d_2}{\varepsilon_2} + \frac{d_3}{\varepsilon_4}\right] - \frac{qN_A d_3^2}{2\varepsilon_4} + \Delta E_c - \Delta E_{F1} - \Delta E_{c34} \qquad \text{(B.60)}$$

$$+ qN_D\left\{\frac{(d_2 - d_1)^2}{2\varepsilon_2} + \frac{(d_3 - d_2)}{K_2} + \frac{(d_1 d_3 - d_3^2)}{\varepsilon_4} + \left[\frac{d_1}{K_2} + \frac{K_1}{(K_2)^2}\right][\ln(K_4)]\right\}$$

$$-V_4(z) = qn_s\left[\frac{1}{K_2}\ln(K_4) - \frac{d_2}{\varepsilon_2} + \frac{d_3}{\varepsilon_4} - \frac{z}{\varepsilon_4}\right] + \Delta E_c - \Delta E_{F1} - \Delta E_{c34}$$

$$+ qN_D\left\{\frac{(d_2 - d_1)^2}{2\varepsilon_2} + \frac{(d_3 - d_2)}{K_2} + \frac{(d_1 d_3 - d_3^2)}{\varepsilon_4}\right. \qquad \text{(B.61)}$$

$$\left. + \left[\frac{d_1}{K_2} + \frac{K_1}{(K_2)^2}\right][\ln(K_4)] - \frac{qN_D(d_1 - d_3)z}{\varepsilon_4}\right\} - \frac{qN_A(z - d_3)^2}{2\varepsilon_4} \quad (d_3 \le z \le d_4)$$

(volts)

Charge-Control Equations

Graded-Layer Enhanced Schottky-Barrier Pseudomorphic MODFET. A charge-control equation is now derived by using (B.61) to relate the 2DEG density (n_s) to the Schottky-barrier potential (ϕ_B) and applied potential (V_G) at the metal gate. The electrostatic potential ($-V_4(d_4)$) at the metal/p^+-GaAs Schottky-barrier interface must be equal to the Schottky-barrier gate potential minus the applied gate potential. Equating the electrostatic potential at the gate to (B.61) at $z = d_4$ yields

$$\phi_B - V_G = -V_4(d_4) \qquad \text{(B.62)}$$

Rearranging (B.62) in terms of n_s and using (2.2) yields

$$n_s = \frac{\varepsilon_2}{q(d^* + \Delta d)}(V_G - V_{OFF}^*) \quad (cm^{-2}) \qquad V_G > V_{OFF}^*$$
$$= 0 \qquad\qquad\qquad\qquad (cm^{-2}) \qquad V_G \le V_{OFF}^* \tag{B.63}$$

where

$$d^* = -\frac{\varepsilon_2}{K_2}\ln(K_4) + d_2 - \frac{d_3\varepsilon_2}{\varepsilon_4} + \frac{d_4\varepsilon_2}{\varepsilon_4} \quad (\text{Å}) \tag{B.64}$$

$$\Delta d = \frac{a\varepsilon_2}{q} \qquad (\text{Å}) \tag{B.65}$$

$$V_{OFF}^* = \phi_B - qN_D\left\{\frac{(d_2 - d_1)^2}{2\varepsilon_2} + \frac{(d_3 - d_2)}{K_2} + \frac{(d_1 d_3 - d_3^2)}{\varepsilon_4} - \frac{(d_1 - d_3)d_4}{\varepsilon_4}\right.$$
$$\left. + \left[\frac{d_1}{K_2} + \frac{K_1}{(K_2)^2}\right][\ln(K_4)]\right\} + \frac{qN_A(d_4 - d_3)^2}{2\varepsilon_4} - \Delta E_c + \Delta E_{F0} + \Delta E_{c34} \tag{B.66}$$

(volts)

The final form for n_s (B.63) is similar to that of Drummond et al. [25] for the normal MODFET (see (2.4) in Chapter II). Thus the standard charge control model can be used for the (ESP)MODFET structure of Fig. B.1 by replacing V_{OFF} with V_{OFF}^* and d with d*.

Graded-Layer Pseudomorphic MODFET. For the case of the pseudomorphic MODFET (Fig. B.1 without a p^+-GaAs layer), the electrostatic potential at the metal/AlGaAs interface is solved as in (B.62) through (B.66). Equating the electrostatic potential at the gate to $-V_3(d_3)$ (e.g. setting $z = d_3$ in (B.54)) yields

$$\phi_B - V_G = - V_3(d_3) \tag{B.67}$$

Rearranging (B.67) in terms of n_s and using (2.2) yields

$$n_s = \frac{\varepsilon_2}{q\left[-\frac{\varepsilon_2}{K_2}\ln(K_4) + d_2 + \Delta d\right]}\left\{ V_G - \phi_B + qN_D\left[\frac{(d_2 - d_1)^2}{2\varepsilon_2} + \left(\frac{d_1}{K_2} + \frac{K_1}{(K_2)^2}\right)[\ln(K_4)] + \frac{(d_3 - d_2)}{K_2}\right]\right\} + \Delta E_c - \Delta E_{F0} \qquad V_G > V_{OFF*}$$

(B.68)

$$= 0 \qquad V_G \le V_{OFF*}$$

which also may be written in the form of (2.4).

Appendix C

Computer Modelling Programs

Program 1

```
10 '***PLOT OF THE CHANGE IN BANDGAP (ΔElh) OF A COMPRESSED InGaAs EPITAXIAL
LAYER
11 '***GROWN COHERENTLY UPON A SUBSTRATE WITH THE InGaAs MOLE FRACTION AS A
PARAMETER.
12 '***WRITTEN BY JAMES A. LOTT 19 AUG 87
20 DIM PLOT1(4), PLOT(3,20):CLS
30 FOR y=0 TO .6 STEP .15
40 C11=11.8-3.551*y:C12=5.38-.854*y:HYDROP=1.15-.15*y
50 a=-(1/3)*(C11+2*C12)*HYDROP:b=-1.7-.1*y
60 K=(-2*a*((C11-C12)/C11)+b*((C11+2*C12)/C11))
70 PLOT1(y/.15)=K
80 PRINT y;K
90 NEXT y
100 FOR R=0 TO 3
110 FOR x=0 TO .02 STEP .001
120 deltaElh=PLOT1(R)*x
130 PLOT(R, x/.001)=deltaElh:PRINT x,deltaElh
140 NEXT x
150 NEXT R
160 OPEN "CLIP:" FOR OUTPUT AS #1
170 FOR s=0 TO 20
180 WRITE #1,s,PLOT(0,s),PLOT(1,s),PLOT(2,s),PLOT(3,s)
190 NEXT s
200 CLOSE #1
210 END
```

Program 2

```
10 '***PLOT OF InGaAs MOLE FRACTION YS InGaAs BANDGAP WHEN GROWN COHERENTLY
11 '***UPON A GaAs SUBSTRATE WITH THE InGaAs MOLE FRACTION AS A PARAMETER.
12 '***WRITTEN BY JAMES A. LOTT 19 AUG 87
20 DIM PLOT1(22),PLOT2(22),PLOT3(22)
30 FOR y=0 TO 1.1 STEP .05
40 p=0
50 a1=5.6533+.4051*y
60 a0=5.6533:b=a0
70 a1eff=a1-a0*p*b
80 STRAIN=(a1eff-a0)/a0
90 C11=11.8-3.551*y:C12=5.38-.854*y:HYDROP=1.15-.15*y
100 a=-(1/3)*(C11+2*C12)*HYDROP:b=-1.7-.1*y
110 deltaElh=(-2*a*((C11-C12)/C11)+b*((C11+2*C12)/C11))*STRAIN
120 Eg=1.423-1.615*y+.555*(y)^2
125 Eg2=Eg+deltaElh
130 PLOT1(y/.05)=STRAIN:PLOT2(y/.05)=Eg:PLOT3(y/.05)=Eg2
140 PRINT y;STRAIN;deltaElh;Eg;Eg2
```

```
150 NEXT y
160 OPEN "CLIP:" FOR OUTPUT AS #1
170 FOR s=0 TO 20
180 WRITE #1,s/20,PLOT1(s),PLOT2(s),PLOT3(s)
190 NEXT s
200 CLOSE #1
210 END
```

Program 3

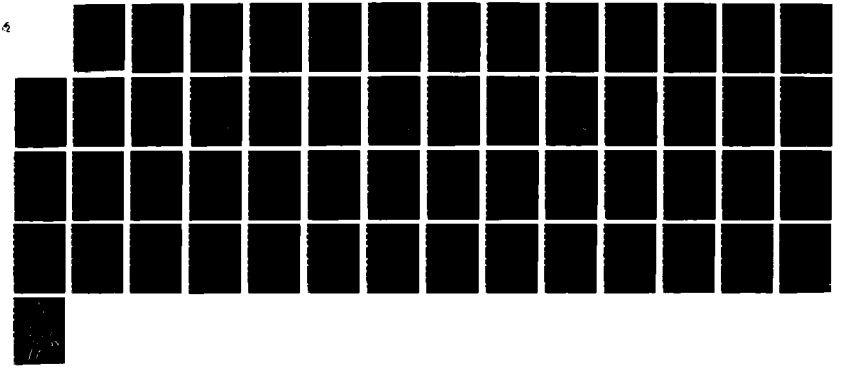
```
10 '******* PLOT OF ELECTRIC FIELD VS. DISTANCE FOR A
MODFET*******ELECTRICFIELD1
20 '*** Written by JAMES A. LOTT 06 MAY 1987 (REVISED 27 August 1987)***
30 '*** program runs on a MACINTOSH™ PLUS***
40 '*** Given Nd,Na,d1-d4,Vb,Vg, program calculates ns and produces (x,y)
50 '*** values for the electric field between the gate and the 2DEG channel
60 '***of a pseudomorphic MODFET and ESPMODFET.
70 DIM PLOT(255),PLOT2(255)
80 CLS
100 E0=8.854E-14:Q=1.602E-19
110 INPUT "Default values (return) or New values (1)";zz
120 INPUT "Device type  GRADED PSEUDO-1  GRADED ESP-_";type
130 X1=.15:Y1=.15:Y2=.15:VGATE=0:Vb=.8:Nd= 2E+18:Na=2E+19
140 IF zz<>1 THEN GOTO 200
145 INPUT "PEAK GRADING Y2";Y2
150 INPUT "metal-semiconductor barrier height Vb";Vb
160 INPUT "gate voltage Vg";VGATE
170 INPUT "n-type doping concentration Nd";Nd
180 IF type=1 THEN GOTO 200
190 INPUT "p-type doping concentration Na";Na
200 INPUT "AlGaAs separation layer thickness d1 (Å)";d1
210 d1=d1*1E-08
220 INPUT "AlGaAs layer thickness dn";dn
230 dn=dn*1E-08:d2=dn+d1
240 INPUT "graded AlGaAs layer thickness dg";dg
250 dg=dg*1E-08:d3=dg+d2
260 INPUT "p+ GaAs layer thickness dp";dp
270 dp=dp*1E-08:d4=dp+d3
300 E1=E0*(13.18-3.12*X1):E2=E1:E3=((13.18-3.12*Y2)*E0+(13.18-3.12*Y1)*E0)/2:E4=13.18*E0
310 deltaEc=.3:deltaEc34=(1.1*Y2):A=1.25E-13:deltad=(A*E2)/Q
320 EFO=0
330 IF type=1 THEN GOTO 500
400 '***routine to determine VOFF & ns for an ESPMODFET
410 VOFF=Vb-((Q*Nd)/(2*E3))*((2*d3*d4*E3)/E4-(2*d1*d4*E3)/E4+d3^2-2*d1*d3+((d2-
d1)^2)*(E3/E2)+2*d1*d2-d2^2+(2*d1*d3*E3)/E4-(2*(d3^2)*E3)/E4)+((Q*Na)/(2*E4))*((d4-d3)^2)-
deltaEc+EFO+deltaEc34
420 ns=(E2/(Q*(deltad+d4*E2/E4+(d3*E2)/E3+d2-(d2*E2)/E3-d3*E2/E4)))*(Vg-VOFF):IF ns<0 THEN
ns=0
430 PRINT VOFF;ns
440 INPUT "Continue?";zz:GOTO 600
500 '***routine to determine VOFF & ns for a pseudomorphic MODFET
510 VOFF=Vb-((Q*Nd)/(2*E3))*(d3^2-2*d1*d3+((d2-d1)^2)*(E3/E2)+2*d1*d2-d2^2)-deltaEc+EFO
520 ns=(E2/(Q*(deltad+(d3*E2)/E3+d2-(d2*E2)/E3)))*(Vg-VOFF):IF ns<0 THEN ns=0
530 PRINT VOFF;ns
540 INPUT "Continue?";zz
```

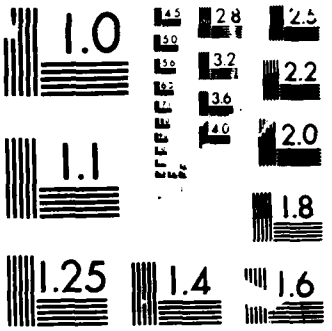
```
600 FOR x=0 TO d4 STEP 5E-08
610 xx=INT(x/5E-08)
620 IF x>d1 THEN GOTO 640
630 ELEC=(Q*ns)/E1:GOTO 700
640 IF x>d2 THEN GOTO 660
650 ELEC=(Q*ns)/E2+((Q*Nd*(d1-x))/E2):GOTO 700
660 IF x>d3 THEN GOTO 680
670 ELEC=(Q*ns)/E3+((Q*Nd*(d1-x))/E3):GOTO 700
680 ELEC=(Q*ns)/E4+((Q*Nd*(d1-d3))/E4)+((Q*Na*(x-d3))/E4)
700 PRINT x,ELEC
710 PLOT(xx)=x:PLOT2(xx)=ELEC
720 NEXT x
800 OPEN "CLIP:" FOR OUTPUT AS # 1
810 FOR s = 0 TO 255
820 WRITE#1,PLOT(s),PLOT2(s)
830 NEXT s
840 CLOSE #1
1000 END
```

Program 4

```
10 '******* PLOT OF ELECTRIC FIELD VS. DISTANCE FOR A GRADED-LAYER
PMODFET*******ELECTRICFIELD2
20 '*** Written by JAMES A. LOTT 20 JUNE1987 (REVISED 27 August 1987)***
30 '*** program runs on a MACINTOSH™ PLUS***
40 '*** Given Nd,Na,d1-d4,Vb,Vg, program calculates ns and produces (x,y)
50 '*** values for the electric field between the gate and the 2DEG channel
60 '***of a graded pseudomorphic MODFET and ESPMODFET.
70 DIM PLOT(255),PLOT2(255)
80 CLS
100 E0=8.854E-14:Q=1.60_E-19
110 INPUT "Default values (return) or New values (1)";zz
120 INPUT "Device type  ES-1 ESP-_";type
130 X1=.15:Y1=.15:Y2=.3:VGATE=0:Vb=.8:Nd= 2E+18:Na=2E+19
140 IF zz<>1 THEN GOTO 200
145 INPUT "PEAK GRADING Y2";Y2
150 INPUT "metal-semiconductor barrier height Vb";Vb
160 INPUT "gate voltage Vg";VGATE
170 INPUT "n-type doping concentration Nd";Nd
180 IF type=1 THEN GOTO 200
190 INPUT "p-type doping concentration Na";Na
200 INPUT "AlGaAs separation layer thickness d1 (Å)";d1
210 d1=d1*1E-08
220 INPUT "AlGaAs layer thickness dn";dn
230 dn=dn*1E-08:d2=dn+d1
240 INPUT "graded AlGaAs layer thickness dg";dg
250 dg=dg*1E-08:d3=dg+d2
260 INPUT "p+ GaAs layer thickness dp";dp
270 dp=dp*1E-08:d4=dp+d3
300 E1=E0*(13.18-3.12*X1):E2=E1:E4=13.18*E0
310 deltaEc=.3:deltaEc34=(1.1*Y2):A=1.25E-13:deltad=(A*E2)/Q
320 EFO=0
330 K1=(13.18-3.12*(Y1-((Y2-Y1)/dg)*d2))*E0
340 K2=-(3.12*((Y2-Y1)/dg))*E0
350 K3=Q*Nd
```

AD-A188 828 CHARACTERIZATION OFEENHANCED SCHOTTKY-BARRIER 3/3
INGAAS/AL(1-X)AS STRINED CH (U) AIR FORCE INST OF TECH
WRIGHT-PATTERSON AFB OH SCHOOL OF ENGI J A LOTT
UNCLASSIFIED DEC 87 AFIT/GE/ENG/87D-38 F/G 9/1 NL





```
360 K4=((K1+K2*d2)/(K1+K2*d3))
370 IF type=1 THEN GOTO 500
400 '***routine to determine VOFF & ns for a Graded Enhanced Schottky-Barrier PMODFET
410 dprime=(-(E2/K2)*(LOG(ABS(K4)))+d2-(d3*E2/E4)+(d4*E2/E4))
420 VOFF=Vb-(Q*Nd)*(((d1*d3-d3^2)/E4)-((d1*d4-d3*d4)/E4)+((((d2-
d1)^2)/(2*E2))+(d1/K2+K1/(K2^2))*(LOG(ABS(K4)))+((d3-d2)/K2))+((Q*Na)/(2*E4))*((d4-d3)^2)-
deltaEc+EFO+deltaEc34
430 ns=((E2)/(Q*(deltad+dprime)))*(VGATE-VOFF):IF ns<0 THEN ns=0
440 PRINT VOFF;ns
450 INPUT "Continue?";zz:GOTO 600
500 '***routine to determine VOFF & ns for a Graded pseudomorphic MODFET
510 dprime=(-(E2/K2)*(LOG(ABS(K4)))+d2)
520 VOFF=Vb-(Q*Nd)*((((d2-d1)^2)/(2*E2))+(d1/K2+K1/(K2^2))*(LOG(ABS(K4)))+((d3-d2)/K2))-
deltaEc+EFO
530 ns=((E2)/(Q*(deltad+dprime)))*(VGATE-VOFF):IF ns<0 THEN ns=0
540 PRINT VOFF;ns
550 INPUT "Continue?";zz
590 '***Routine to determine xy values for the Electric Field for the PMODFET
600 FOR x=0 TO d4 STEP 5E-08
610 xx=INT(x/5E-08)
620 IF x>d1 THEN GOTO 640
630 ELEC=(Q*ns)/E1:GOTO 700
640 IF x>d2 THEN GOTO 660
650 ELEC=(Q*ns)/E2+((Q*Nd*(d1-x))/E2):GOTO 700
660 IF x>d3 THEN GOTO 680
665 E3=K1+K2*x
670 ELEC=(Q*ns)/E3+((Q*Nd*(d1-x))/E3):GOTO 700
680 ELEC=(Q*ns)/E4+((Q*Nd*(d1-d3))/E4)+((Q*Na*(x-d3))/E4)
700 PRINT x,ELEC
710 PLOT(xx)=x:PLOT2(xx)=ELEC
720 NEXT x
800 OPEN "CLIP:" FOR OUTPUT AS # 1
810 FOR s = 0 TO 255
820 WRITE#1,PLOT(s),PLOT2(s)
830 NEXT s
840 CLOSE #1
1000 END
```

Program 5

```
10 '*** GRADED-LAYER PMODFET PROGRAM ***GRADED PMODFET1
20 '***Written by JAMES A. LOTT 1 April 1987 (Revised 23 Aug 1987)***
30 '***Program runs on a MACINTOSH™ PLUS***
40 '***Determines xy coordinates for energy band diagram plot***
50 '***An effective permittivity in Region III is assumed***
90 DIM PLOT(255),PLOT2(255)
100 CLS
110 E0=8.854E-14
120 Q=1.602E-19
125 INPUT "Device type GRADED PSEUDO-1 GRADED ESP-_";type
130 '***test vectors*:X1=.15:Y1=.15:Y2=.3:Vg=0:Vb=.8:Nd= 2E+18:Na=1E+19:GOTO 200
140 INPUT "mole fraction of Al (d1≤x≤d2)";X1
150 INPUT "graded mole fraction of Al x=d2";Y1
160 INPUT "graded mole fraction of Al x=d3";Y2
170 INPUT "metal-semiconductor barrier height Vb";Vb
```

```
175 INPUT "gate voltage Vg";Vg
180 INPUT "n-type doping concentration Nd";ND:EF2=(.69)*(.0259)*(LOG(ND/1.8E+17))
185 'IF type=1 THEN GOTO 200
190 INPUT "p-type doping concentration Na";Na
200 INPUT "AlGaAs separation layer thickness d1 (Å)";d1
210 d1=d1*1E-08
220 INPUT "AlGaAs layer thickness dn";dn
230 dn=dn*1E-08:d2=dn+d1
240 INPUT "graded AlGaAs layer thickness dg";dg
250 dg=dg*1E-08:d3=dg+d2
255 'IF type=1 THEN GOTO 300
260 INPUT "p+ GaAs layer thickness dp";dp
270 dp=dp*1E-08:d4=dp+d3
300 E1=E0*(13.18-3.12*X1)
310 E2=E1
315 E3=((13.18-3.12*Y2)*E0+(13.18-3.12*Y1)*E0)/2:'***effective permittivity
320 E4=13.18*E0
350 K1=(13.18-3.12*(Y1-((Y2-Y1)/dg)*d2))*E0
360 K2=-(3.12*((Y2-Y1)/dg))*E0
370 K3=Q*ND
380 K4=((K1+K2*d2)/(K1+K2*d3))
390 deltaEc=.3
400 deltaEc34= (1.1*Y2)
405 a=1.25E-13
410 deltad=(a*E2)/Q
440 EFO=0
480 IF type<>1 THEN GOTO 900
500 '***routine to determine VOFF & ns for the pseudomorphic (P) MODFET
510 VOFF=Vb-((Q*ND)/(2*E3))*(d3^2-2*d1*d3+((d2-d1)^2)*(E3/E2)+2*d1*d2-d2^2)-deltaEc+EFO
520 ns=(E2/(Q*(deltad+(d3*E2)/E3+d2-(d2*E2)/E3)))*(Vg-VOFF):IF ns<0 THEN ns=0
580 PRINT VOFF;ns
590 INPUT "ok?";zz
600 '***ENERGY BAND POTENTIAL VS. DISTANCE FOR PMODFET
610 z=0:EFI=(a)*ns +EFO
620 FOR z = 0 TO d3 STEP 5E-08
630 IF z >= d1 THEN GOTO 670
640 PSI1 = -(Q*ns*z)/E1 +deltaEc -EFI
650 PRINT z;PSI1:PLOT((d4-z)/5E-08)=z:PLOT2((d4-z)/5E-08)=PSI1
660 GOTO 800
670 IF  z>=d2 THEN GOTO 710
680 PSI2 = -(Q*ns*z)/E2 +((Q*ND)*((z-d1)^2))/(2*E2) +deltaEc - EFI
690 PRINT z;PSI2::PLOT((d4-z)/5E-08)=z:PLOT2((d4-z)/5E-08)=PSI2
700 GOTO 800
710 PSI3 =-((Q*ns)/E2)*((z*E2/E3)+d2-(d2*E2/E3))+((Q*ND)/(2*E3))*((z^2)-(2*d1*z)+(((d2-
d1)^2)*E3/E2)+(2*d1*d2)-d2^2) + deltaEc - EFI
730 PRINT z;PSI3:PLOT((d4-z)/5E-08)=z:PLOT2((d4-z)/5E-08)=PSI3
800 NEXT z
810 GOTO 1210
900 '***routine to determine VOFF & ns for ESPMODFET
910 VOFF=Vb-((Q*ND)/(2*E3))*((2*d3*d4*E3)/E4-(2*d1*d4*E3)/E4+d3^2-2*d1*d3+((d2-
d1)^2)*(E3/E2)+2*d1*d2-d2^2+(2*d1*d3*E3)/E4-(2*(d3^2)*E3)/E4)+((Q*Na)/(2*E4))*((d4-d3)^2)-
deltaEc+EFO+deltaEc34
920 ns=(E2/(Q*(deltad+d4*E2/E4+(d3*E2)/E3+d2-(d2*E2)/E3-d3*E2/E4)))*(Vg-VOFF):IF ns<0 THEN
ns=0
980 PRINT VOFF;ns
990 INPUT "ok?";zz
1000 '***ENERGY BAND  POTENTIAL VS. DISTANCE FOR THE GRADED-LAYER PMODFET
```

```
1010 z=0:EFI=(a)*ns +EFO
1020 FOR z = 0 TO d4 STEP 5E-08
1030 IF z >= d1 THEN GOTO 1070
1040 PSI1 = -(Q*ns*z)/E1 +deltaEc -EFI
1050 PRINT z;PSI1:PLOT((d4-z)/5E-08)=z:PLOT2((d4-z)/5E-08)=PSI1
1060 GOTO 1200
1070 IF z>=d2 THEN GOTO 1110
1080 PSI2 = -(Q*ns*z)/E2 +((Q*ND)*((z-d1)^2))/(2*E2) +deltaEc - EFI
1090 PRINT z;PSI2::PLOT((d4-z)/5E-08)=z:PLOT2((d4-z)/5E-08)=PSI2
1100 GOTO 1200
1110 IF z>=d3 THEN GOTO 1160
1120 PSI3 =-((Q*ns)/E2)*((z*E2/E3)+d2-(d2*E2/E3))+((Q*ND)/(2*E3))*((z^2)-(2*d1*z)+(((d2-
d1)^2)*E3/E2)+(2*d1*d2)-d2^2) + deltaEc - EFI
1140 PRINT z;PSI3:PLOT((d4-z)/5E-08)=z:PLOT2((d4-z)/5E-08)=PSI3
1150 GOTO 1200
1160 PSI41=((Q*ND)/(2*E3))*((2*d3*z*E3)/E4-(2*d1*z*E3)/E4+d3^2-2*d1*d3+((d2-
d1)^2)*(E3/E2)+2*d1*d2-d2^2+(2*d1*d3*E3)/E4-(2*(d3^2)*E3)/E4)-((Q*Na)/(2*E4))*((z-d3)^2)
1170 PSI42=-((Q*ns)/E2)*(z*E2/E4+(d3*E2)/E3+d2-(d2*E2)/E3-d3*E2/E4)
1180 PSI4 = PSI41+PSI42-deltaEc34+deltaEc-EFI
1190 PRINT z;PSI4:PLOT((d4-z)/5E-08)=z:PLOT2((d4-z)/5E-08)=PSI4
1200 NEXT z
1210 OPEN "CLIP:" FOR OUTPUT AS # 1
1220 FOR s = 0 TO 255
1230 WRITE#1,PLOT(s),PLOT2(s)
1240 NEXT s
1250 CLOSE #1
2000 END
```

Program 6

```
10 '*** GRADED-LAYER PMODFET PROGRAM ***GRADED PMODFET2***e(z)
20 '***Written by JAMES A. LOTT 17 June 1987 (REVISED 25 August 1987)***
30 '***program runs on a MACINTOSH™ PLUS***
40 '***Determines xy coordinates for energy band diagram plot***
50 '***Assumes a permittivity in REGION III that varies with position***
90 DIM PLOT(255),PLOT2(255)
100 CLS
110 E0=8.854E-14
120 Q=1.602E-19
125 INPUT "Device type GRADED PSEUDO-1 GRADED ESP-_";type
130 '***test vectors*:X1=.15:Y1=.15:Y2=.3:VGATE=0:Vb=.8:Nd= 2E+18:Na=1E+19:GOTO 200
140 INPUT "mole fraction of Al (d1≤x≤d2)";X1
150 INPUT "graded mole fraction of Al x=d2";Y1
160 INPUT "graded mole fraction of Al x=d3";Y2
170 INPUT "metal-semiconductor barrier height Vb";Vb
175 INPUT "gate voltage Vg";VGATE
180 INPUT "n-type doping concentration Nd";Nd
185 'IF type=1 THEN GOTO 200
190 INPUT "p-type doping concentration Na";Na
200 INPUT "AlGaAs separation layer thickness d1 (Å)";d1
210 d1=d1*1E-08
220 INPUT "AlGaAs layer thickness dn";dn
230 dn=dn*1E-08:d2=dn+d1
240 INPUT "graded AlGaAs layer thickness dg";dg
250 dg=dg*1E-08:d3=dg+d2
```

```
255 'IF type=1 THEN GOTO 300
260 INPUT "p+ GaAs layer thickness dp";dp
270 dp=dp*1E-08:d4=dp+d3
300 E1=E0*(13.18-3.12*X1)
310 E2=E1
320 E4=13.18*E0
350 K1=(13.18-3.12*(Y1-((Y2-Y1)/dg)*d2))*E0
360 K2=-(3.12*((Y2-Y1)/dg))*E0
370 K3=Q*Nd
380 K4=((K1+K2*d2)/(K1+K2*d3))
390 deltaEc=.3
400 deltaEc34= (1.1*Y2)
405 a=1.25E-13
410 deltad=(a*E2)/Q
440 EFO=0
480 IF type<>1 THEN GOTO 900
500 '***routine to determine VOFF & ns for the pseudomorphic (P) MODFET
510 dprime=(-(E2/K2)*(LOG(ABS(K4)))+d2)
530 VOFF=Vb-(Q*Nd)*((((d2-d1)^2)/(2*E2))+(d1/K2+K1/(K2^2))*(LOG(ABS(K4)))+((d3-d2)/K2))-
deltaEc+EFO
540 ns=((E2)/(Q*(deltad+dprime)))*(VGATE-VOFF)
580 PRINT VOFF;ns:IF ns<0 THEN ns=0
590 INPUT "ok?";zz
600 '***ENERGY BAND POTENTIAL VS. DISTANCE FOR PMODFET
610 z=0:EFI=(a)*ns +EFO:IF EF1=0 THEN EF1=VOFF-EFO
620 FOR z = 0 TO d3 STEP 5E-08
630 IF z >= d1 THEN GOTO 670
640 PSI1 = -(Q*ns*z)/E1 +deltaEc -EFI
650 PRINT z;PSI1:PLOT((d4-z)/5E-08)=z:PLOT2((d4-z)/5E-08)=PSI1
660 GOTO 800
670 IF z>=d2 THEN GOTO 710
680 PSI2 = -(Q*ns*z)/E2 +((Q*Nd)*((z-d1)^2))/(2*E2) +deltaEc - EFI
690 PRINT z;PSI2::PLOT((d4-z)/5E-08)=z:PLOT2((d4-z)/5E-08)=PSI2
700 GOTO 800
710 K5 = LOG(ABS((K1+K2*d2)/(K1+K2*z)))
720 PSI3 =(Q*ns)*(K5/K2-d2/E2)+(Q*Nd)*((((d2-d1)^2)/(2*E2))+(d1/K2+K1/(K2^2))*(K5)+((z-d2)/K2)) +
deltaEc - EFI
730 PRINT z;PSI3:PLOT((d4-z)/5E-08)=z:PLOT2((d4-z)/5E-08)=PSI3
800 NEXT z
810 GOTO 1210
900 '***routine to determine VOFF & ns for ESPMODFET
910 dprime=(-(E2/K2)*(LOG(ABS(K4)))+d2-(d3*E2/E4)+(d4*E2/E4))
920 VOFF=Vb-(Q*Nd)*(((d1*d3-d3^2)/E4)-((d1*d4-d3*d4)/E4)+(((d2-
d1)^2)/(2*E2))+(d1/K2+K1/(K2^2))*(LOG(ABS(K4)))+((d3-d2)/K2))+((Q*Na)/(2*E4))*((d4-d3)^2)-
deltaEc+EFO+deltaEc34
930 ns=((E2)/(Q*(deltad+dprime)))*(VGATE-VOFF):IF ns<0 THEN ns=0
980 PRINT VOFF;ns
990 INPUT "ok?";zz
1000 '***ENERGY BAND POTENTIAL VS. DISTANCE FOR THE GRADED-LAYER PMODFET
1010 z=0:EFI=(a)*ns +EFO:IF EF1=0 THEN EF1=VOFF-EFO
1020 FOR z = 0 TO d4 STEP 5E-08
1030 IF z >= d1 THEN GOTO 1070
1040 PSI1 = -(Q*ns*z)/E1 +deltaEc -EFI
1050 PRINT z;PSI1:PLOT((d4-z)/5E-08)=z:PLOT2((d4-z)/5E-08)=PSI1
1060 GOTO 1200
1070 IF z>=d2 THEN GOTO 1110
1080 PSI2 = -(Q*ns*z)/E2 +((Q*Nd)*((z-d1)^2))/(2*E2) +deltaEc - EFI
```

```
1090 PRINT z;PSI2::PLOT((d4-z)/5E-08)=z:PLOT2((d4-z)/5E-08)=PSI2
1100 GOTO 1200
1110 IF z>=d3 THEN GOTO 1160
1120 K5 = LOG(ABS((K1+K2*d2)/(K1+K2*z)))
1130 PSI3 =(Q*ns)*(K5/K2-d2/E2)+(Q*Nd)*((((d2-d1)^2)/(2*E2))+(d1/K2+K1/(K2^2))*(K5)+((z-d2)/K2)) +
deltaEc - EFI
1140 PRINT z;PSI3:PLOT((d4-z)/5E-08)=z:PLOT2((d4-z)/5E-08)=PSI3
1150 GOTO 1200
1160 PSI41=(Q*Nd)*(((d1*d3-d3^2)/E4)-((d1*z-d3*z)/E4)+(((d2-
d1)^2)/(2*E2))+(d1/K2+K1/(K2^2))*(LOG(ABS(K4)))+((d3-d2)/K2))-((Q*Na)/(2*E4))*((z-d3)^2)
1170 PSI42 =(Q*ns)*((1/K2)*(LOG(ABS(K4)))-d2/E2+(d3/E4)-(z/E4))
1170 PSI4 = PSI41+PSI42-deltaEc34+deltaEc-EFI
1180 PRINT z;PSI4:PLOT((d4-z)/5E-08)=z:PLOT2((d4-z)/5E-08)=PSI4
1200 NEXT z
1210 OPEN "CLIP:" FOR OUTPUT AS # 1
1220 FOR s = 0 TO 255
1230 WRITE#1,PLOT(s),PLOT2(s)
1240 NEXT s
1250 CLOSE #1
2000 END
```

Program 7

```
1 '***GRADED-LAYER ESPMODFET ENERGY BAND DIAGRAM: CLASSICAL MODEL 3
2 '***WRITTEN BY JAMES A. LOTT  SEPT 87
10 CLS
90 DIM u(6,251),Ev(6,250),nplot(6,251),pplot(6,251),ND(6),NA(6),
deltaEc(6),Eg(6),e(6),d(7)
100 FOR R = 1 TO 6:READ d(R):NEXT R
120 FOR R = 1 TO 6: READ NA(R):NEXT R
130 FOR R = 1 TO 6:READ ND(R):NEXT R
150 READ X1,X2,Y1,vb,Vg
160 DATA 100,100,250,30,150,250
170 DATA  2E19,1E14,1E14,1E14,1E14,1E14
180 DATA  0,2E18,2E18,0,0,0
190 DATA  0.15,0.30,0.15,0.8,0
200 GOSUB 300:'*** INITIALIZATION
210 GOSUB 700:'*** POISSON SOLVER
220 GOSUB 3100:'***CALCULATE VALENCE BAND PLOT POINTS
230 GOSUB 3200:'*** LOAD PLOT DATA INTO CLIPBOARD
250 END
300 '***************INITIALIZATION SUBROUTINE*******************
310 '*******CONSTANTS
320 e0=8.85418D-14
330 K=8.617E-05
340 T=300
350 q=1.602E-19
360 Nc=4.7E+17
370 Nv=7E+18
380 '******PERMITTIVITY
390 e(6)=13.18*e0:'GaAs
400 e(5)=(13.18+1.42*Y1)*e0:'InGaAs
410 e(4)=(13.18-3.12*X1)*e0:'AlGaAs
420 e(3)=e(4):'AlGaAs
430 e(2)=(e(4)+(13.18-3.12*X2)*e0)/2:'AlGaAs Graded
```

```
440 e(1)=13.18*e0:'GaAs
450 '******ENERGY BANDGAP
460 Eg(6)=1.424:'GaAs
470 Eg(5)=(1.424-1.615*Y1+.555*(Y1^2)):'InGaAs Strained
480 Eg(4)=1.424+1.247*X1:'AlGaAs
490 Eg(3)=Eg(4):'AlGaAs
500 Eg(2)=1.424+1.247*X2:'AlGaAs max
510 Eg(1)=1.424:'GaAs
520 '******CONDUCTION BAND DISCONTINUITY USING 65:35 RULE
530 deltaEc(5)=(Eg(6)-Eg(5))*.65:'InGaAs/GaAs
540 deltaEc(4)=(Eg(5)-Eg(4))*.65:'AlGaAs/InGaAs
550 deltaEc(1)=(Eg(2)-Eg(1))*.65:'GaAs/AlGaAs
560 deltaEc(2)=0:deltaEc(3)=0:deltaEc(6)=0
570 '******BULK VALUE OF CONDUCTION BAND z=W
580 VcBW=(K*T)*(LOG(NA(6)/Nv))+Eg(6)
590 RETURN
600 '****************END INITIALIZATION SUBROUTINE****************
610 '
700 '***************** POISSON SOLVER SUBROUTINE ****************
710 '*** NUMERICAL SOLUTION
720 h=1E-08:' FINITE DIFFERENCE OF 1Å
730 u(1,0)=vb
740 u(1,1)=vb+.01795425#:'*** initial guess
750 FOR z = 2 TO (d(1)+1)
760 Ec=u(1,z-1):EG1=Eg(1)
770 GOSUB 3000:nplot(1,z-1)=n:pplot(1,z-1)=p
780 R=(ND(1)-NA(1)+p-n):'PRINT p;n
790 u(1,z)=(h^2)*(q*R/e(1))-u(1,z-2)+2*(u(1,z-1)):'***PRINT u(1,z);z
800 NEXT z
810 FOR L = 2 TO 6
820 u(L,0)=u(L-1,d(L-1)) + deltaEc(L-1):'***PRINT u(L,0)
830 Ec=u(L,0):EG1=Eg(L)
840 GOSUB 3000:nplot(L,0)=n:pplot(L,0)=p
850 R=(ND(L)-NA(L)+p-n)
860 uu1=(h^2)*(q*R/e(L))
870 KK=(u(L-1,d(L-1)+1)-u(L-1,d(L-1)-1))*(e(L-1)/e(L))
880 uu2=2*(u(L,0))
890 u(L,1)=(uu1 + KK + uu2)/2:'***PRINT u(L,1):'STOP
900 FOR z = 2 TO (d(L)+1)
910 Ec=u(L,z-1):EG1=Eg(L):IF L=2 THEN GOSUB 3050
920 GOSUB 3000:nplot(L,z-1)=n:pplot(L,z-1)=p
930 R=(ND(L)-NA(L)+p-n)
940 u(L,z)=(h^2)*(q*R/e(L))-u(L,z-2)+2*(u(L,z-1)):'***PRINT u(L,z);z;nplot(L,z-1);pplot(L,z-1)
950 NEXT z
960 NEXT L
961 STOP:GOTO 1050
970 u0=u(6,249):u1=u(6,250)
980 FOR z = 251 TO 5001
990 Ec=u1:EG1=Eg(6):GOSUB 3000
1000 R=(ND(6)-NA(6)+p-n)
1010 u2=(h^2)*(q*R/e(6))-u0+2*u1:'***PRINT u2;z
1020 IF z = 5000 THEN GOTO 1040:IF u2>=VcBW THEN STOP
1030 u0=u1:u1=u2
1040 NEXT z
1041 STOP
1050 RETURN
1200 '****************END POISSON SOLVER SUBROUTINE*************
```

```
1210 '
3000 '******SUB DETERMINES THE CONCENTRATION OF FREE CARRIERS******
3010 n=Nc*(EXP(-Ec/(.02585)))
3020 p=Nv*(EXP((Ec-EG1)/(.02585)))
3030 RETURN
3050 '*******SUB ACCOUNTS FOR A GRADED BANDGAP IN REGION II********
3060 delX=X1-X2: d2=(d(1)+d(2)) : dg=d(2)
3070 EG1=1.424+1.247*(delX*(z+d(1))/dg+X1-(delX*d2/dg))
3080 RETURN
3100 '*******SUB DETERMINES POINTS FOR VALENCE BAND PLOT**********
3110 FOR L = 1 TO 6
3120 FOR z = 0 TO d(L) STEP 5
3130 EG1=Eg(L):IF L=2 THEN GOSUB 3050
3140 Ev(L,z)=u(L,z)-EG1:PRINT Ev(L,z)
3150 NEXT z
3160 NEXT L
3170 RETURN
3200 '*******SUBROUTINE LOADS PLOT POINTS INTO CLIPBOARD**********
3210 OPEN "CLIP:" FOR OUTPUT AS # 3
3220 FOR L = 1 TO 6
3230 FOR z = 0 TO (d(L)-5) STEP 5
3240 WRITE#3, z;u(L,z);Ev(L,z);ND(L);NA(L);nplot(L,z);pplot(L,z)
3241 'PRINT z;u(L,z);Ev(L,z);ND(L);NA(L);nplot(L,z);pplot(L,z)
3250 NEXT z
3260 NEXT L
3270 CLOSE #3
3280 RETURN
```

Appendix D

MODFET Fabrication Procedure

This appendix describes the procedures that were used to fabricate (ESP)MODFET structures from MBE-grown substrates. The substrates were prepared by the University of Illinois, Coordinated Sciences Laboratory [34]. The procedures listed below are based on those developed over many years at the University of Illinois, and on those used by McLaughlin [60].

Sample Cutting

Epitaxial Layers were grown on GaAs substrates (the surface areas were approximately 2.5 cm^2). The substrates were scribed into four distinct samples using a diamond tip chisel. Each scribed sample measured approximately 1 cm^2. Before processing, the sample was inspected under a microscope for surface imperfections.

Indium Removal

The indium solder that was used to mount the GaAs substrates to a molybdenum holder before MBE-growth was removed as follows:

Step 1. A solution of mercuric chloride (1 gram $HgCl_2$) in 10 ml N,N-dimethyl formamide ($HCON(CH_3)_2$) was prepared.

Step 2. The sample was immersed in a small plastic beaker of the mercuric chloride solution. The beaker was placed in an ultrasonic tank and agitated for 15-20 seconds; this was repeated twice.

Step 3. The sample was removed from the solution and rinsed with methanol from a squeeze bottle. This removed large particles of indium. Before re-immersing in the solution, the sample was rinsed in deionized water (DIW).

Step 4. After about 5 minutes in the solution, all indium was removed from the backside of the sample. It was again rinsed in methanol, followed by DIW.

Step 5. The top surface of the sample was cleaned using a soft cotton swab dipped in a solution of Alconox cleaner. This removed any $HgCl_2$ that remained on the surface.

Step 6. The sample was thoroughly rinsed in DIW and dried with dry nitrogen.

Lapping

A protective coating of photoresist was spun on the front surface of the sample. The back side of the sample was then thinned to a thickness of about 400 μm.

Step 1. The sample was placed on a glass slide and baked at 110 °C for 5 minutes to dry the surface.

Step 2. The sample was removed from the oven and placed on the photoresist spinner. The sample was spun at 5000 rpm and dry nitrogen was sprayed on the surface to remove surface particles.

Step 3. Several drops of AZ-1350SF photoresist (unfiltered) were placed on the sample's surface. The sample was spun at 5000 rpm for 30 seconds.

Step 4. The sample was placed on a glass slide and baked at 110 °C for 30 minutes. This hardened the photoresist.

Step 5. The sample was mounted on a lapping block. The block was first heated on a hot plate. Paraffin (clear wax) was melted on the surface and the sample placed on the block, crystal growth (shinny) side down.

Step 6. Powered 5 μm dry grit (aluminum oxide powder) was placed on a lapping surface (glass plate) and DIW added to create a slurry mixture. The inverted lapping block

was placed on the lapping surface. Using a figure-eight motion with the lapping block, the back surface of the sample was lapped away. Periodic checks were made with a micrometer (difference measurements) until the desired thickness (≈ 400 μm) was reached.

Step 7. The sample was rinsed in DIW to remove lapping grit. It was then removed from the lapping block by reheating the block on a hot plate, melting the paraffin.

Step 8. Paraffin was removed from the sample with a stream of trichloroethane (TCE) from a squeeze bottle. The protective photoresist was then removed with an acetone spray. The sample was cleaned in methanol (stream) and DIW (stream), and blown dry with nitrogen.

Standard p^+-GaAs Epitaxial Layer Etch

The following is the standard procedure used to etch the p^+-GaAs surface epitaxial layer. The procedure was used to etch away the entire GaAs surface layer on a few of the samples and also to remove the parasitic MESFET path between gate and source, and gate and drain of the enhanced Schottky-barrier samples.

Step 1. A solution of NH_4OH:H_2O_2:DIW in a concentration of 3:1:150 by volume was carefully and cautiously mixed.

Step 2. The sample was placed in this solution for 3.5 seconds. A GaAs etch rate of 30 Å/sec was assumed [34].

Mesa Etch

This procedure was used to define mesas of active material by etching defined portions of the sample down to the GaAs substrate. The active material mesas isolate the MODFETs.

Step 1. The sample was dried for 5 minutes at 110 °C to remove surface moisture.

Step 2. The sample was again placed on the photoresist spinner and coated with the AZ 1350J (filtered) photoresist. The sample was spun at 5000 rpm for 30 seconds.

Step 3. The sample was baked at 90 °C for 20 minutes.

Step 4. The sample was aligned under the mesa etch mask and exposed under ultraviolet light (UV) for 6 seconds.

Step 5. The sample was developed in 5:1, DIW: AZ 351 developer for 50 seconds and rinsed in DIW.

Step 6. The sample was placed in a beaker of 3:1:1, DIW:H_2O_2:HF for 8 seconds. This etched the sample down to the GaAs buffer layer in order to isolate regions of active material.

Step 7. The sample was rinsed thoroughly in DIW to stop the etch.

Step 8. The positive photoresist was stripped in acetone. The sample was then cleaned in methanol and DIW, and blown dry with nitrogen.

Source and Drain Contact

Source and drain ohmic contacts were formed in a two step process. Metal was first evaporated onto the surface. Transient annealing was then used to form the ohmic contacts.

Metallization.

Step 1. The sample was baked at 110 °C for 5 minutes to remove surface moisture.

Step 2. AZ 1350J (filtered) photoresist was applied and the sample was spun for 30 seconds at 5000 rpm.

Step 3. The sample was softbaked at 90 °C for 20 minutes.

Step 4. The photoresist was thickest at the edges of the sample, and had to be removed there. Black paper cutouts were made just smaller than the sample. The cutouts were placed

over the sample in the mask aligner and the edge photoresist exposed to UV for 30 seconds. The photoresist was developed in 5:1, DIW:AZ 351 developer for 30 seconds.

Step 5. The sample was placed in the mask aligner and aligned under the source and drain contact mask. The sample was exposed for 6 seconds to UV light.

Step 6. The photoresist was developed in 5:1, DIW:AZ 351 for 50 seconds.

Step 7. The sample was placed into the evaporation chamber, which was then pumped down to approximately 1×10^{-6} Torr.

Step 8. Contact metal was evaporated (thermally(AuGe) and by electron-beam(Ni)) , beginning with 400 Å AuGe. A Sloan digital thickness monitor was used to monitor the metal thicknesses. Next, 110 Å of Ni was evaporated, followed by 600 Å of Au.

Step 9. The samples were allowed to cool for 15 minutes before the evaporation chamber was brought up to atmospheric pressure.

Step 10. Metal was lifted-off with an acetone soak. The sample was placed in an ultrasonic bath, three times for 15 seconds, to agitate and dissolve the photoresist.

Source and Drain Alloying to Form Ohmic Contacts.

Step 1. The alloying oven was stabilized at 500 °C.

Step 2. The sample was placed in a quartz boat and loaded into the sample tube at the end of the oven.

Step 3. The oven was purged with hydrogen gas (nonreactive environment that removes oxygen) for 3 minutes. This time also allowed samples at the end of the sample tube to slowly come up to temperature.

Step 4. A quartz boat with a sample was pushed into the oven and annealed for 50 seconds.

Step 5. The quartz boat was pulled back out to the edge of the tube to cool for 3 minutes.

Step 6. The quartz boat was removed from the oven and then the sample was removed from the quartz boat.

Gate Metallization

The procedure used to apply the Schottky-barrier gate was as follows:

Step 1. The sample was baked for 5 minutes at 110 °C.

Step 2. Filtered AZ 4110 positive photoresist was applied and spun for 30 seconds at 5000 rpm.

Step 3. The sample was re-baked at 70 °C for 20 minutes to promote photoresist adhesion.

Step 4. Photoresist was exposed and developed at the edges of the sample as discussed above.

Step 5. The sample was placed in the mask aligner and aligned under the gate mask. The photoresist was exposed for 7.5 seconds (all exposures were at a power setting of 8.7 mW/cm^2).

Step 6. The sample was soaked in chlorobenzene (C_6H_5Cl) for 15 minutes.

Step 7. The sample was post-baked in a 90 °C oven for 10 minutes.

Step 8. The photoresist was developed for 60 seconds in 7:2 DIW:AZ 400K developer.

Step 9. The sample was soaked for 20 seconds in a "descumming" solution (1:10, NH_4OH:DIW) to remove photoresist from the gate region.

Step 10. The sample was rinsed in DIW and dried with nitrogen.

Step 11. The sample was placed in the evaporation chamber which was then pumped down to approximately 10^{-6} Torr.

Step 12. Approximately 300 nm of aluminum was thermally evaporated onto the samples to form the gate contact.

Step 13. Samples were cooled for 15 minutes before opening the metallization chamber to atmospheric pressure.

Step 14. The photoresist and metal were lifted-off with an acetone soak. The beaker was placed in the ultrasonic tank and agitated for up to 10 seconds. The lift-off process took about 5 minutes.

Step 15. The sample was rinsed in DIW and dried with nitrogen.

Step 16. The enhanced Schottky-Barrier samples were all put through the standard p^+-GaAs layer etch at this point, as described above.

Overlay Metallization

Thicker metal was evaporated onto the regions of the contact pads where bond wires would later be attached. This provided a durable surface for Au wire bonding.

Step 1. The process used here was exactly the same as for gate metallization, with one exception. A different mask was used to allow metallization on source, gate and drain pads, but only in the areas where thick bond wires could be attached.

Step 2. At this point, the samples were ready for post-fabrication DC testing, dicing, microstripline carrier mounting, and then onto microwave performance testing.

Appendix E

Plotted DC and Microwave Data

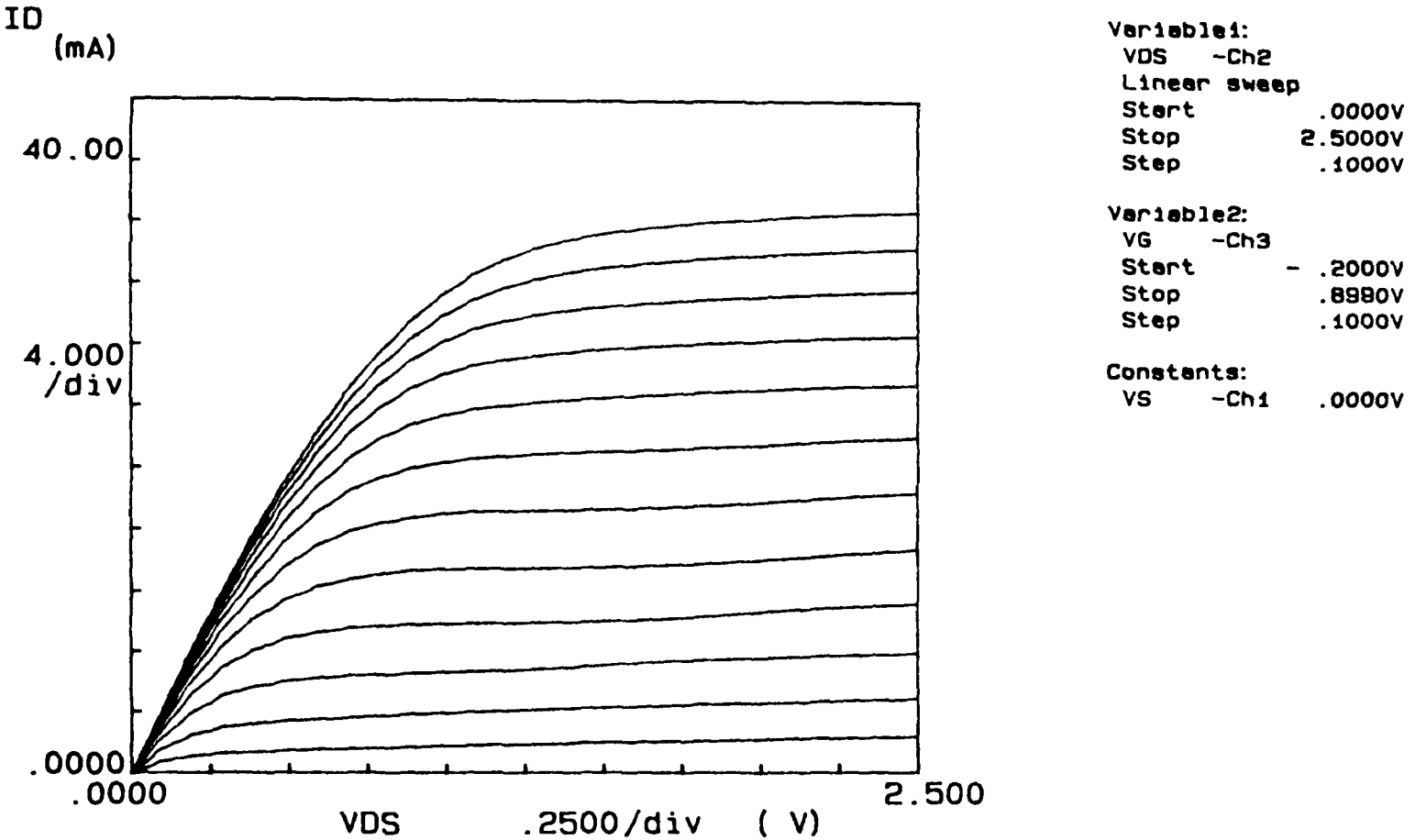


Fig. E.1 Plot of I_D vs. V_{DS} for Sample 3379A (Graded)

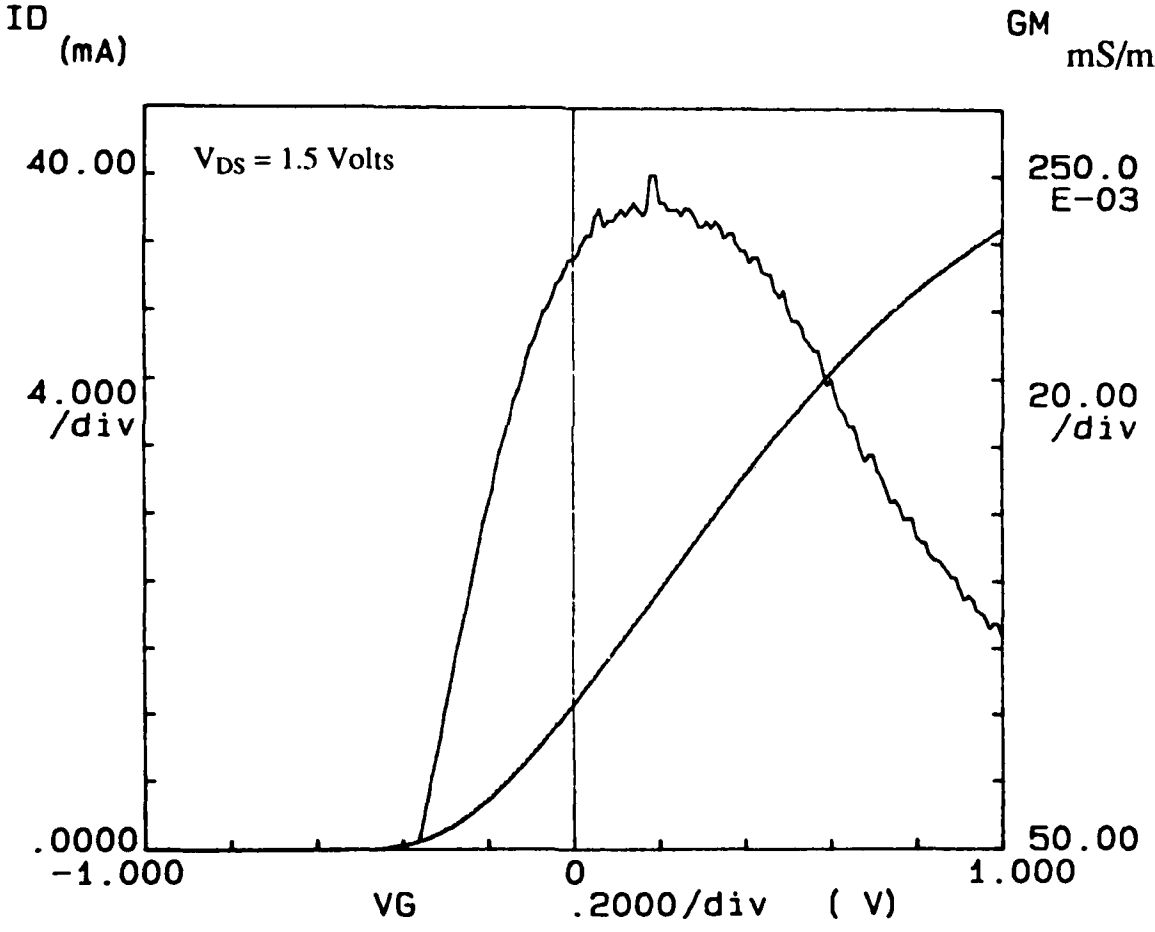


Fig. E.2 Combined Plot of I_D vs. V_{GS} and g_m vs. V_{GS} (with V_{DS} = 1.5 V) for Sample 3379A (Graded)

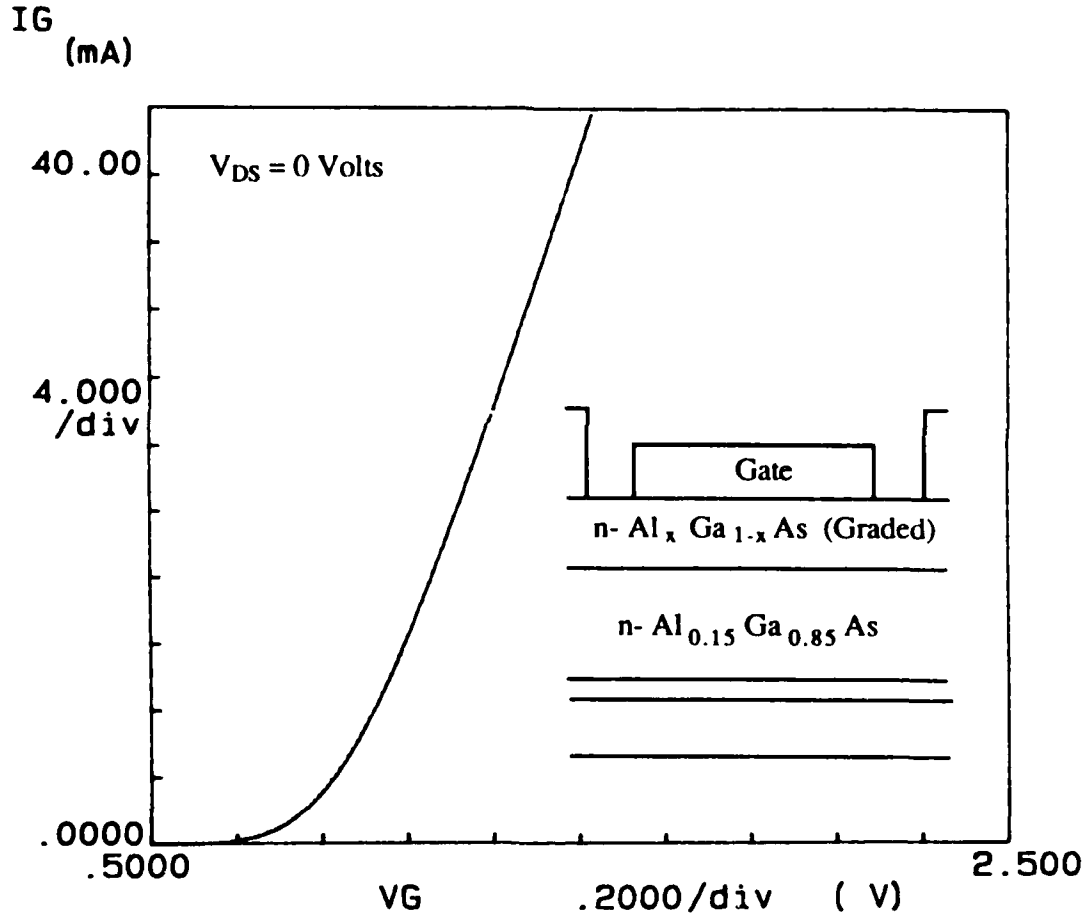


Fig. E.3 Plot of I_G vs. V_{GS} (with V_{DS} = 0 V) for Sample 3379A (Graded)

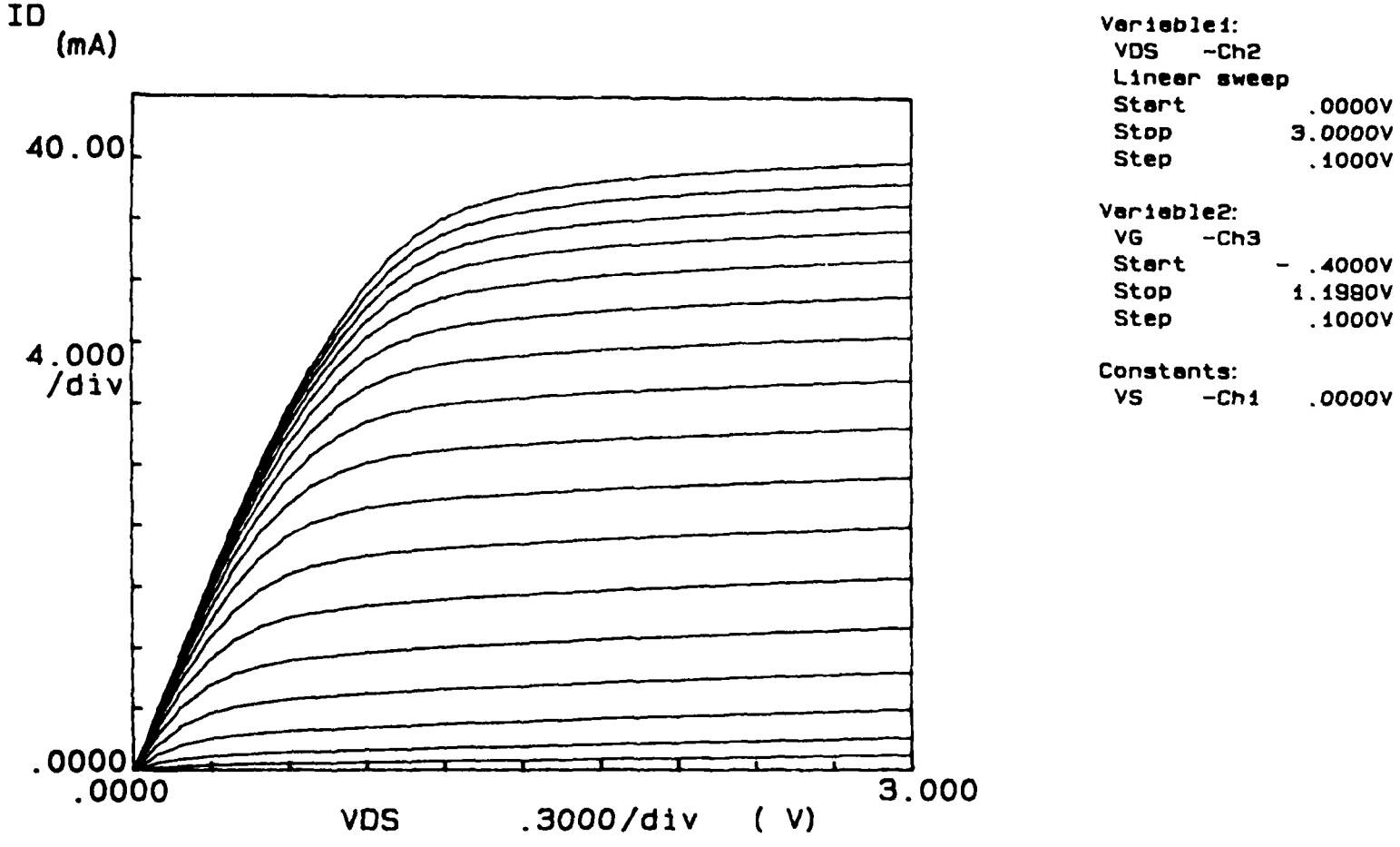


Fig. E.4 Plot of I_D vs. V_{DS} for Sample 3408A (Ungraded)

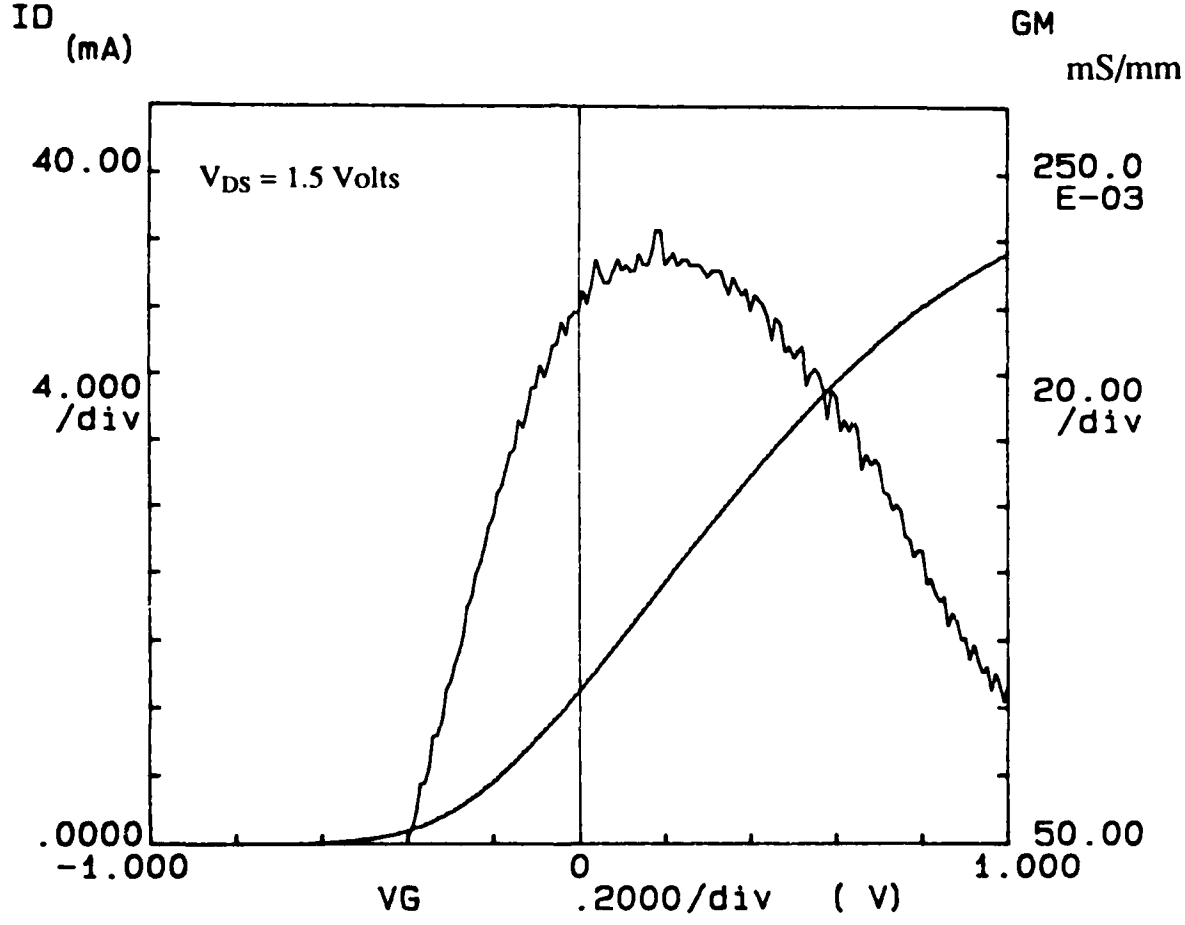


Fig. E.5 Combined Plot of I_D vs. V_{GS} and g_m vs. V_{GS} (with V_{DS} = 1.5 V) for Sample 3408A (Ungraded)

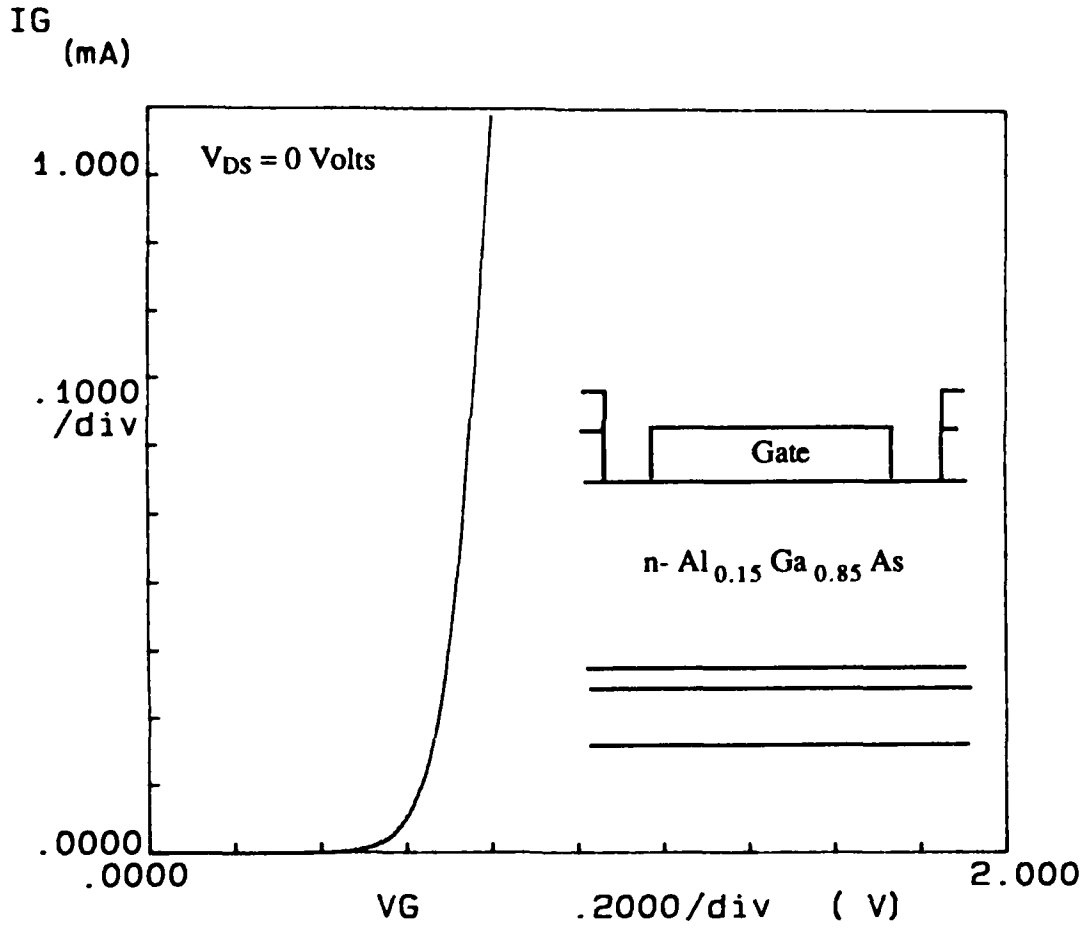


Fig. E.6 Plot of I_G vs. V_{GS} (with V_{DS} = 0 V) for Sample 3408A (Ungraded)

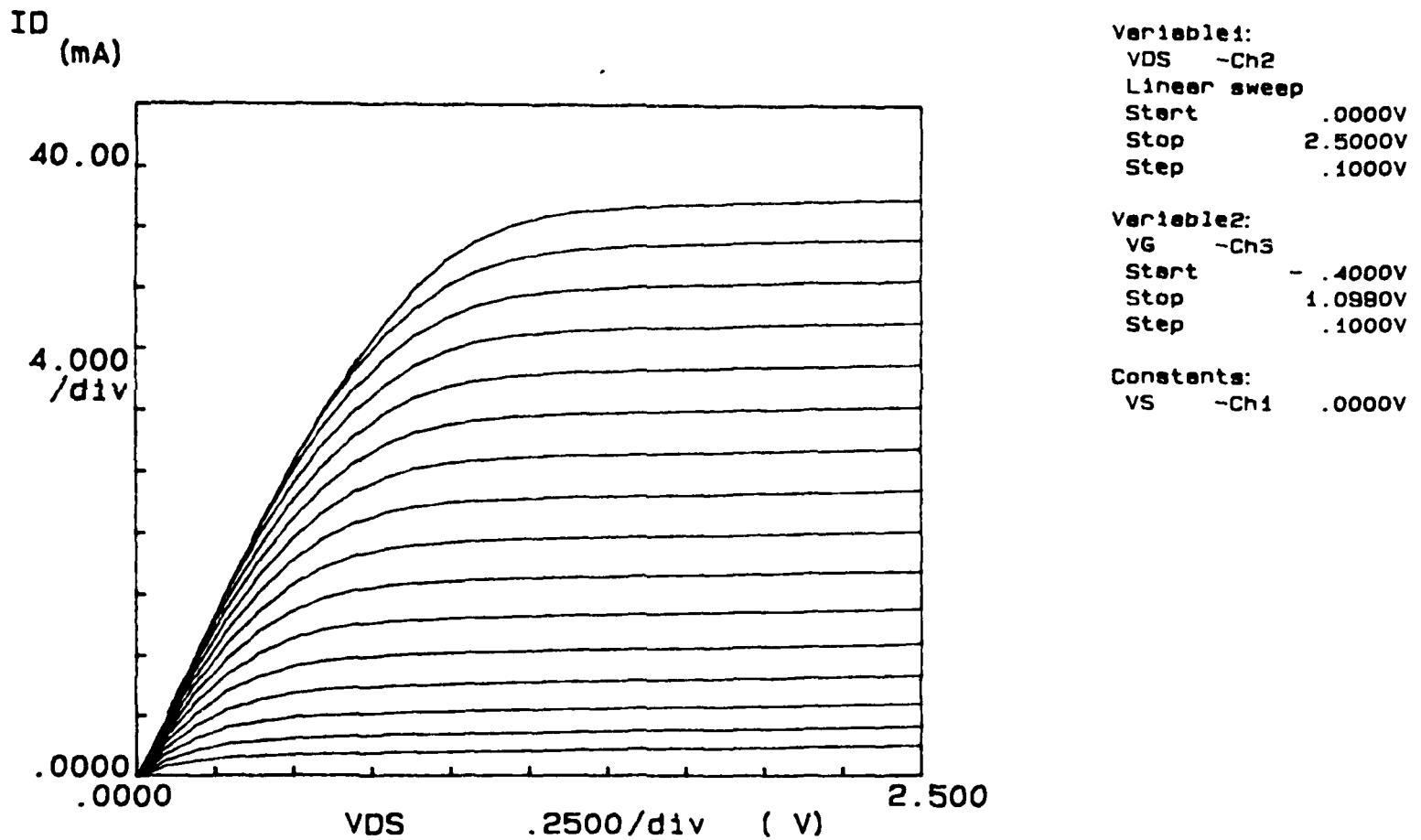


Fig. E.7 Plot of I_D vs. V_{DS} for Sample 3408D (p^+-Ungraded)

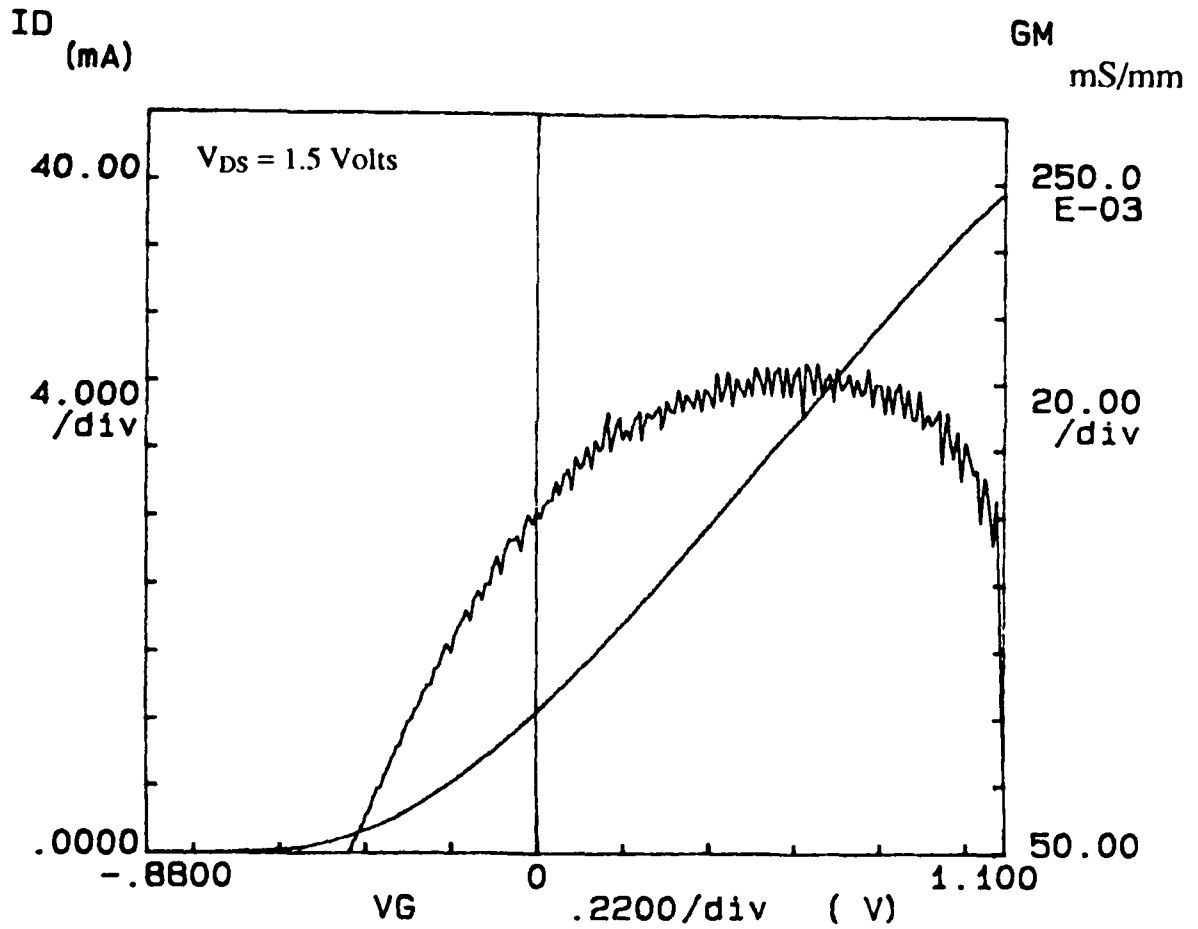


Fig. E.8 Combined Plot of I_D vs. V_{GS} and g_m vs. V_{GS} (with V_{DS} = 1.5 V) for Sample 3408D (p^+-Ungraded)

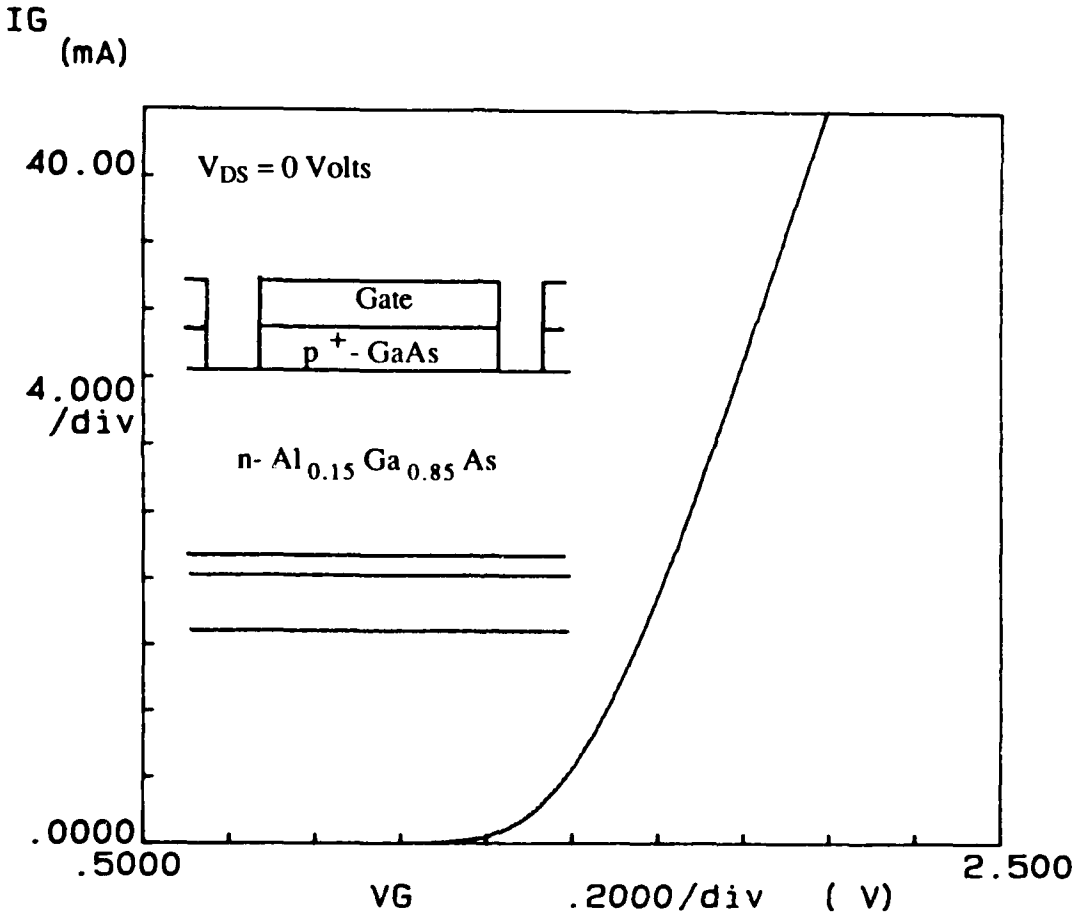


Fig. E.9 Plot of I_G vs. V_{GS} (with V_{DS} = 0 V) for Sample 3408D (p^+-Ungraded)

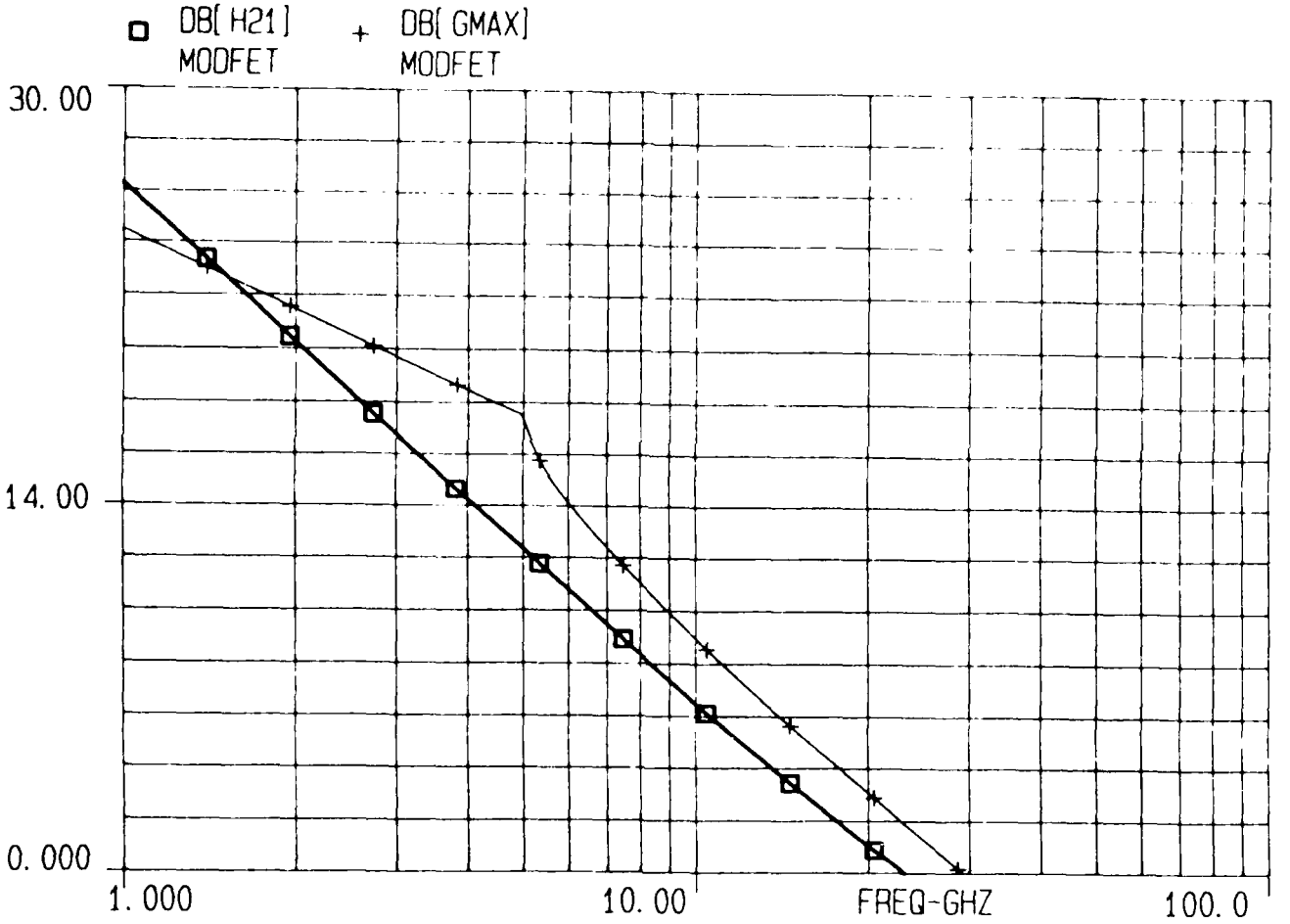


Fig. E.10 Plot of the Maximum Available Gain (G_{max}) and Forward Current Gain ($20\log|h_{21}|$) vs. Frequency for Sample 3379A (Graded)

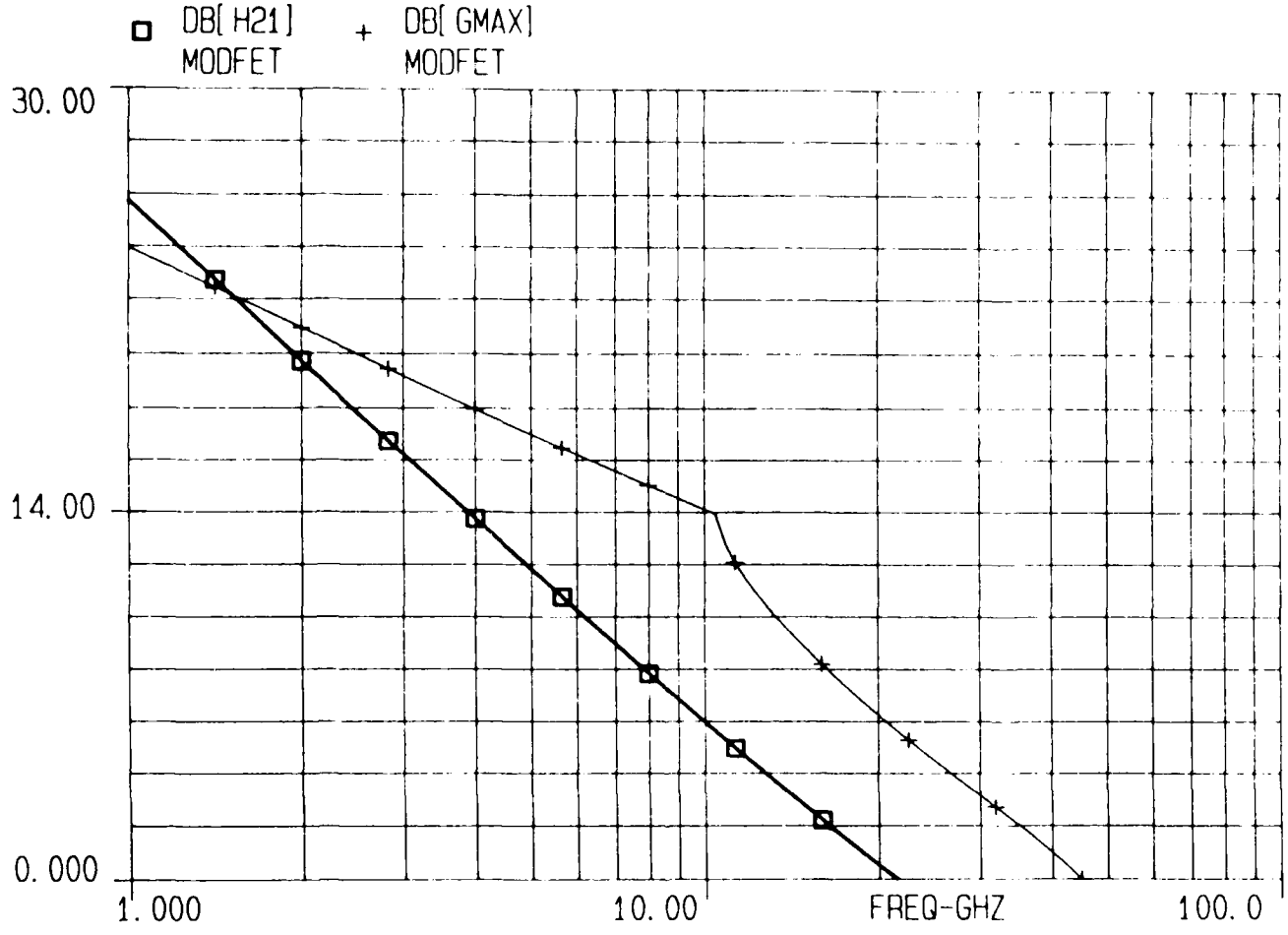


Fig. E.11 Plot of the Maximum Available Gain (G_{max}) and Forward Current Gain ($20\log|h_{21}|$) vs. Frequency for Sample 3379C (p^+-Graded)

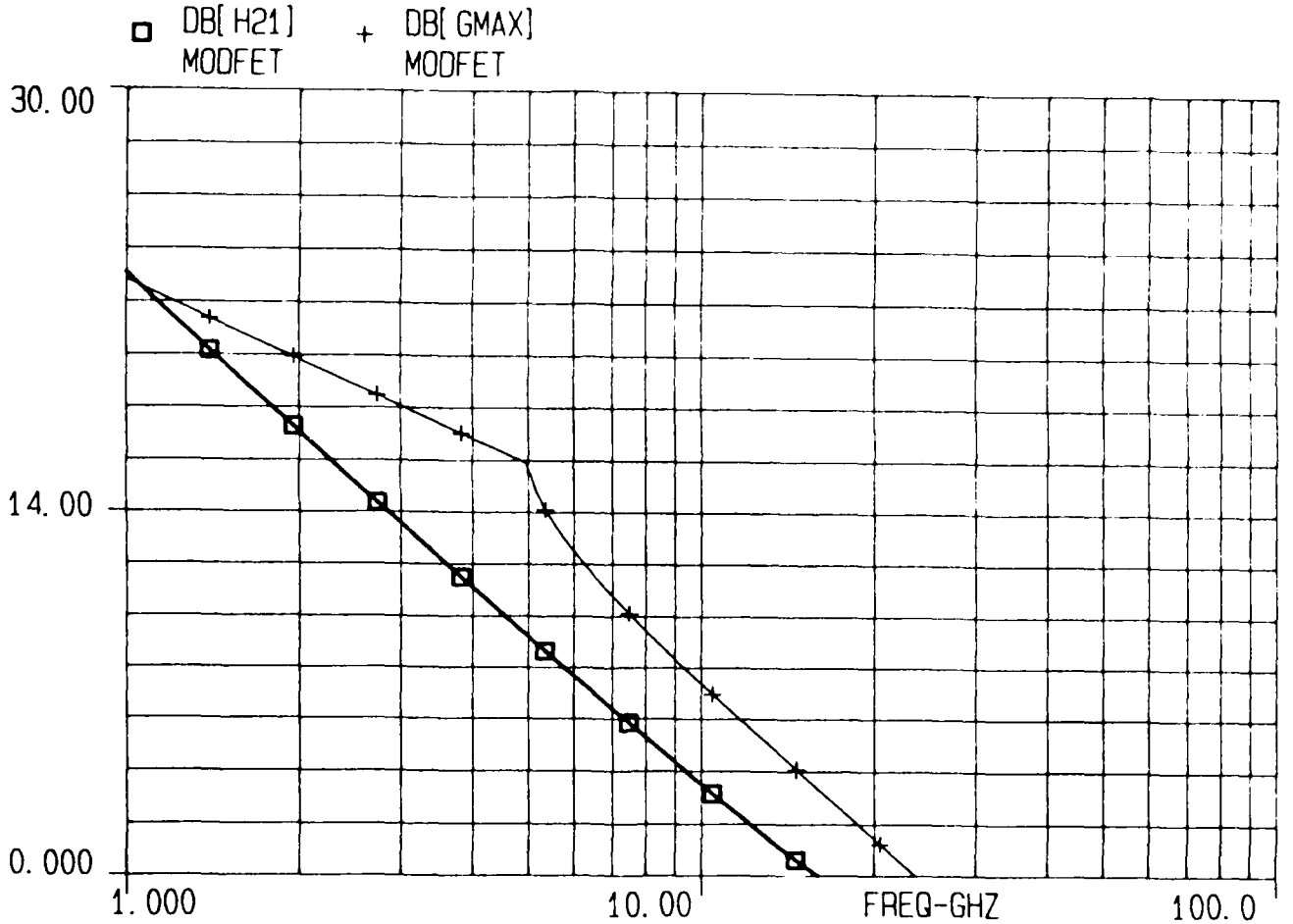


Fig. E.12 Plot of the Maximum Available Gain (G_{max}) and Forward Current Gain ($20\log|h_{21}|$) vs. Frequency for Sample 3408A (Ungraded)

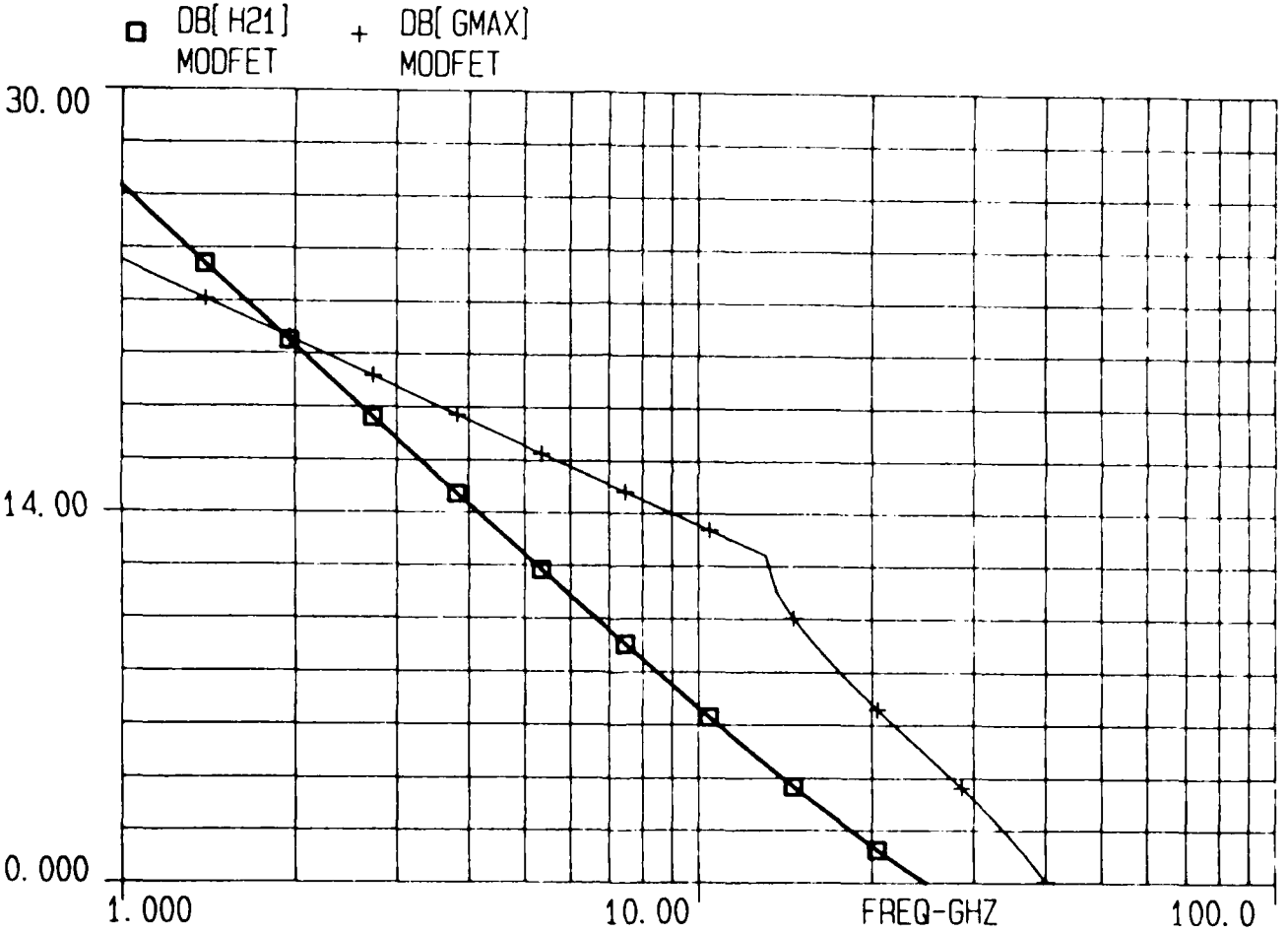


Fig. E.13 Plot of the Maximum Available Gain (G_{max}) and Forward Current Gain ($20\log|h_{21}|$) vs. Frequency for Sample 3408D (p^+-Ungraded)

Appendix F

Classical and Quantum Mechanical Charge-Control Models for n-Type Strained Channel MODFETs

The general purpose charge-control model developed by Jaffe [43; 44] at The University of Michigan will be outlined. The model was modified by Jaffe for the author and applied to the (ESP)MODFETs fabricated in this study [42]. The results are compared to the models developed in Appendices A and B (Models 1 and 2) and discussed in Chapter V. Also, a revised classical charge-control model (Model 3) was formulated (based on a numerical solution of Poisson's equation) and will be presented in this appendix. Model 3 is an improvement over Models 1 and 2 because it accounts for free holes and electrons. The four charge-control models were used to provide an accurate estimation of the energy band diagram (and thus the effective Schottky-barrier height) for the MODFET structures in this study. In addition, Models 1 and 2 were used to estimate the MODFET's threshold voltage and quantum-confined charge-density (n_s).

The Charge-Control Model Developed by The University of Michigan

The charge-control model uses a self-consistent solution of the Poisson equation and the Schrödinger wave equation. A finite-difference numerical technique (vectorized Newton method) is used with standard eigen-system solution routines [44]. First, Poisson's equation is solved using classical charge statistics (neglecting quantum charge confinement). This solution is then used as the starting point for the complete quantum mechanical solution. A tight-binding model is used, along with the virtual crystal approximation for alloys, to simulate the changes on the bandgap and effective masses of

the strained-channel material [44]. The model uses a 65:35 rule for conduction:valence band discontinuities. This means that at a given hetero-interface, ΔE_c is given by $0.65\Delta E_g$ and ΔE_v is given by $0.35\Delta E_g$, where ΔE_g is the bandgap difference of the two materials.

The calculated energy bandgap of strained $In_yGa_{1-y}As$ lattice matched to a GaAs substrate is shown in Table F.1. Also shown is the unstrained case. Strain reduces the

Table F.1

Bandgaps and Electron Effective Masses in

Pseudomorphically Strained Channel Material [44]

	$In_yGa_{1-y}As$				
y	$E_{g\text{-unstrained}}$	$E_{g\text{-strained}}$	$m^*_{unstrained}$	$m^*_{\parallel strained}$	$m^*_{\perp\ strained}$
0.00	1.4540	1.4540	0.0660	0.0660	0.0660
0.03	1.4211	1.4337	0.0648	0.0656	0.0652
0.06	1.3881	1.4132	0.0636	0.0651	0.0646
0.09	1.3552	1.3924	0.0624	0.0647	0.0639
0.12	1.3223	1.3714	0.0612	0.0642	0.0634

crystal symmetry of $In_yGa_{1-y}As$ from cubic to tetragonal [44]. This means that the electron effective mass in the gamma valley (single and nondegenerate) will be different in directions parallel and perpendicular to the crystal growth direction. However, this effect is small, as shown in Table F.1. The problem is much more complicated for the p-channel MODFET, since the hole band structure is comprised of two degenerate bands [44].

The charge-control model begins with the one-dimensional Poisson equation [42]:

$$\nabla^2 V(z) = -\frac{\rho(z)}{\varepsilon(z)} \qquad \text{(F.1)}$$

The charge profile in the MODFET is given by [42]

$$\rho(z) = N_D(z) - N_A(z) - n_{free}(z) + p_{free}(z) - \sum_i n_i \psi_i^*(z)\psi_i(z) \quad (cm^{-3}) \qquad \text{(F.2)}$$

where

N_D = donor doping level (cm^{-3})

N_A = acceptor doping level (cm^{-3})

n_{free} = free electron concentration (cm^{-3})

p_{free} = free hole concentration (cm^{-3})

$\sum_i n_i \psi_i^*(z)\psi_i(z)$ = quantum confined charge distribution of the i^{th} sub-band (cm^{-3})

n_i = electron concentration in the i^{th} sub-band (cm^{-3})

ψ_i = normalized wave function of the i^{th} sub-band (unitless)

Both models use the "pseudomorphic approximation" for strain incorporation in the channel material; stated by Jaffe as follows [43]:

> The lattice constant of the regions matched to the substrate is unaffected. In the non-matched region, the parallel lattice constant is forced to take on the value of the lattice constant of the substrate, while the perpendicular lattice constant of the non-matched material is then altered according to the Poisson effect.

Justification for this assumption was presented in Chapter 3.

Classical Charge Statistics Model. In this model, the last term in (F.2) (the quantum confined charge distribution) is not considered. Instead, the free electron and free hole concentrations are used to account for the quantum confined charge, using Fermi-Dirac statistics. The density of free states is calculated in the traditional way using conduction and

valence band effective masses. (For the quantum mechnical calculation, the three dimensional density of states is assumed to begin at the top of the confining potential (E_B), instead of the conduction band).

For a (nearly) parabolic band structure, and using the Maxwell-Boltzmann approximation (e.g. $E_c - E_F > 3kT$), the concentration of free electrons and holes is given by [42; 83:75]

$$n = N_c \exp[(E_F - E_c)/kT] \qquad (cm^{-3}) \qquad \text{(F.3a)}$$

$$p = N_v \exp[(E_c - E_g - E_F)/kT] \qquad (cm^{-3}) \qquad \text{(F.3b)}$$

where the effective density of states in the conduction (N_C) and valence (N_v) bands are given by [83:75]

$$N_c = 2\left(\frac{2\pi kTm_e^*}{h^2}\right)^{3/2} \qquad (cm^{-3}) \qquad \text{(F.4a)}$$

$$N_v = 2\left(\frac{2\pi kTm_h^*}{h^2}\right)^{3/2} \qquad (cm^{-3}) \qquad \text{(F.4b)}$$

and m_e^* and m_h^* are the effective masses of electrons and holes, respectively. Thus, classically, the energy band structure of a strained-layer n-type MODFET can be determined by solving (F.1) using (F.2) (quantum charge ignored), (F.3), appropriate boundary conditions, and the bandgap change of the strained-channel. The change of the strained-channel electron effective mass, since it is small (about 5 percent for an InAs mole fraction of 0.10 [44]), may be neglected. Additionally, instead of using the Maxwell-Boltzmann approximation to the Fermi-Dirac distribution function, a look-up table or

numerical technique may be implemented in the computer simulation. This becomes essential at low temperatures.

Quantum Charge Statistics Model. This model is based on a self-consistent solution of Schrödinger's and Poisson's equations. A finite-difference numerical eigenvalue technique is used so that Schrödinger's equations may be solved for arbitrarily-shaped potential wells, and different material parameters across interfaces [43]. An arbitrarily-shaped potential well is shown in Fig. F.1. The free electron charge (n_{free}) is only considered above E_B, and from (F.3a) is given by

$$n_{free} = N_c \exp[(E_F - E_B)/kT] \qquad (cm^{-3}) \qquad (F.5)$$

Below E_B, the time independent (one-dimensional) Schrödinger equation is used to model electrons in the gamma valley of the strained-channel (including parts of the neighboring epitaxial layers to account for the probability that the wave functions will penetrate outside the potential well).

Assuming that the electrons are free in the two directions parallel to the hetero-interface, and assuming parabolic sub-bands with an effective mass $m_{e_{||}}^*$ (different in different epitaxial regions), Schrödinger's equation reduces to [42]

$$-\frac{\hbar^2}{2m_z^*}\nabla^2\psi_i(z) + V(z)\psi_i(z) = E_i\psi_i(z) \qquad (F.6)$$

where

m_z^* = effective electron mass perpendicular to the heterointerface

$V(z)$ = potential profile determined from the solution to Poisson's equation

E_i = eigenenergies; energy level of the i^{th} sub-band.

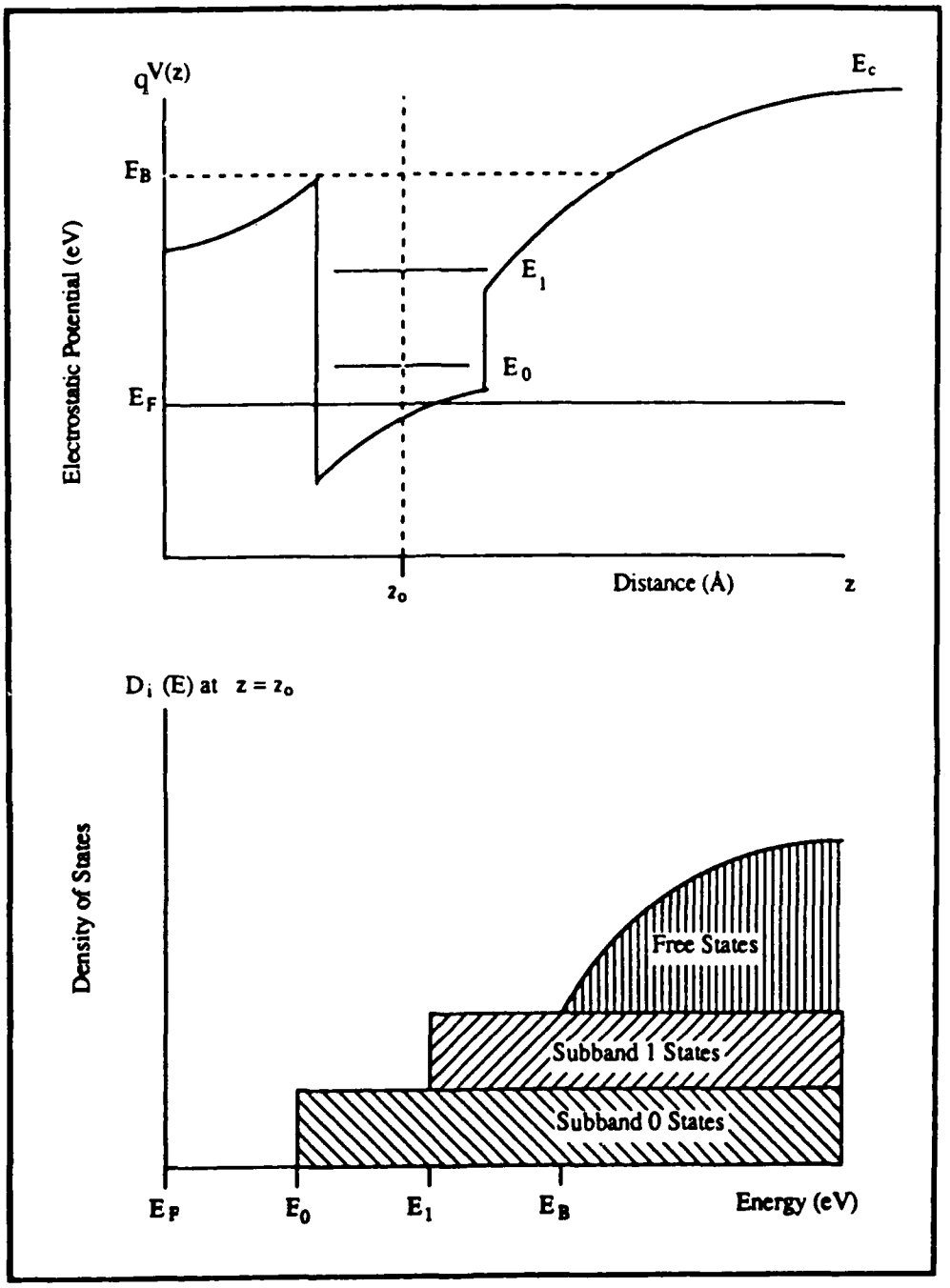


Fig. F.1 A Quantum Potential Well and the Density of States at a Point Inside the Quantum Potential Well. Note that the Free States Begin at an Energy Just Above the Confining Potential [44]

The density of states in each sub-band is a constant and is determined by the parallel effective electron mass. The occupation of each sub-band is determined by integrating the density of states (D(E)) multiplied by the Fermi distribution function (f(E)). The density of electrons in the i^{th} sub-band is then [21; 42]

$$n_i = \int_{E_i}^{\infty} D_i f(E) dE \qquad \text{(F.7a)}$$

This integral is solved by using the substitution $x = (E - E_F)/kT$ in the following formula [21]:

$$\int \frac{dx}{1 + e^{x}} = - \ln(1 + e^{-x})$$

with the result

$$n_i = \frac{m_{\|}^*}{\pi \hbar^2} kT \ln\left[1 + \exp\left(\frac{E_F - E_i}{kT} \right) \right] \qquad \text{(F.7b)}$$

where

$$D_i = \frac{m_{\|}^*}{\pi \hbar^2} \qquad \text{(F.7c)}$$

and $m_{\|\, i}^*$ is taken as an expectation value given by

$$m_{\|i}^* = \frac{\int_{-\infty}^{\infty} \psi_i^*(z)\psi_i(z)m_{\|}^*(z)dz}{\int_{-\infty}^{\infty} \psi_i^*(z)\psi_i(z)dz} \qquad \text{(F.7d)}$$

and $m_{\|\,i}^*$ varies from region to region. After solving for n_i in (F.7), one obtains the quantum confined charge density of the i^{th} subband from

$$\rho_i(z) = n_i\psi_i^*(z)\psi_i(z) \qquad \text{(F.8)}$$

where $\psi_i^*(z)\psi_i(z)$ is the normalized probability of electron occupancy (probability density of finding the particle described by $\psi_i(z)$ [7:168]). Figure F.1 depicts the distribution of free and confined electron states at a position within a quantum potential well.

A Classical Charge-Control Model for the (ESP)MODFET

A revised charge-control model is presented (Model 3). The model is similar to Models 1 and 2 developed in Appendices A and B, respectively. In this model, the free hole and electron concentrations will be given by (F.3), rather than by taking the 2DEG density as an infinitely thin sheet charge and by using (2.2) to model the $\Delta E_{F1}(n_s)$ dependence. All boundary conditions remain unchanged. A numerical finite-difference technique [10: 563-576; 48:847-859] is used to solve Poisson's equation. The result is energy band and charge distribution diagrams based on the material parameters of the given MODFET structure.

Poisson's equation in one-dimension (z) is [48:847]

$$\nabla^2 V(z) = V_{zz}(z) = f(z) \qquad \text{(F.9)}$$

where V(z) is the potential and the subscripts represent partial derivatives (e.g. $V_{zz}(z) = \partial^2 V/\partial z^2$), and $f(z) = \rho(z)/\varepsilon(z)$ is a function of z. The partial derivatives in (F.9) are replaced by corresponding difference quotients and expanded in a Taylor series giving [48:848]

$$V(z+h) = V(z) + hV_z(z) + \frac{1}{2}h^2V_{zz}(z) + \frac{1}{6}h^3V_{zzz}(z) + \ldots \qquad \text{(F.10a)}$$

$$V(z-h) = V(z) - hV_z(z) + \frac{1}{2}h^2V_{zz}(z) - \frac{1}{6}h^3V_{zzz}(z) + \ldots \qquad \text{(F.10b)}$$

where h is a small change in z. By subtracting (F.10b) from (F.10a) and neglecting terms in $h^3, h^4, \ldots$, and solving for $V_z(z)$, the following is obtained [48:848]:

$$\frac{dV}{dz} = V_z(z) \approx \frac{1}{2h}[V(z+h) - V(z-h)] \qquad \text{(F.11a)}$$

or

$$V(z+h) - V(z-h) = 2hV_z(z) \qquad \text{(F.11b)}$$

By adding (F10a) and (F.10b) and neglecting terms in $h^4, h^5, \ldots$, and solving for $V_{zz}(z)$, one obtains [48:848]

$$\frac{d^2V}{dz^2} = V_{zz}(z) \approx \frac{1}{h^2}[V(z+h) - 2V(z) + V(z-h)] \qquad \text{(F.12)}$$

By substituting (F.12) into (F.9) one obtains

$$V(z+h) + V(z-h) - 2V(z) = h^2f(z) \qquad \text{(F.13a)}$$

or

$$V(z+h) = h^2f(z) - V(z-h) + 2V(z) \qquad \text{(F.13b)}$$

which is a difference equation corresponding to (F.9). The goal is to solve (F.13) in a bounded region R ($0 \leq z \leq L$) as shown in Fig. F.2. Within R, one selects a finite number of mesh points P_n =(nh) where n = L/h. With this notation for each mesh point, (F.13b) may be written

$$
\begin{aligned}
P_0: &\quad V_0 = V \text{ (V is given by the boundary condition)} \\
P_1: &\quad V_1 = h^2 f(V_o) - V_{-1} + 2V_o \\
P_2: &\quad V_2 = h^2 f(V_1) - V_o + 2V_1 \\
P_3: &\quad V_3 = h^2 f(V_2) - V_1 + 2V_2 \qquad \text{(F.14)} \\
&\quad \bullet \\
&\quad \bullet \\
&\quad \bullet \\
P_n: &\quad V_n = h^2 f(V_{n-1}) - V_{n-2} + 2V_{n-1}
\end{aligned}
$$

Letting P_0 (z = 0) correspond to the gate metal/top epitaxial layer interface, one obtains $V_0 = \phi_B$ (Schottky-barrier height) from the required boundary condition. Let P_n (z = L) correspond to the point in the GaAs (the GaAs buffer layer or further into the GaAs substrate) beneath the $In_{0.15}Ga_{0.85}As$ strained channel layer, at which the conduction band reaches its equilibrium value. In other words, the point at which the GaAs is no longer depleted of carriers and the electric field equals zero. This point will be called W. At z = W the potential $V_n = E_c - E_F$ is given by [90:23]

$$V_n = E_c - E_F = kT \ln(N_A/N_v) + E_g \quad \text{(eV)} \qquad \text{(F.15)}$$

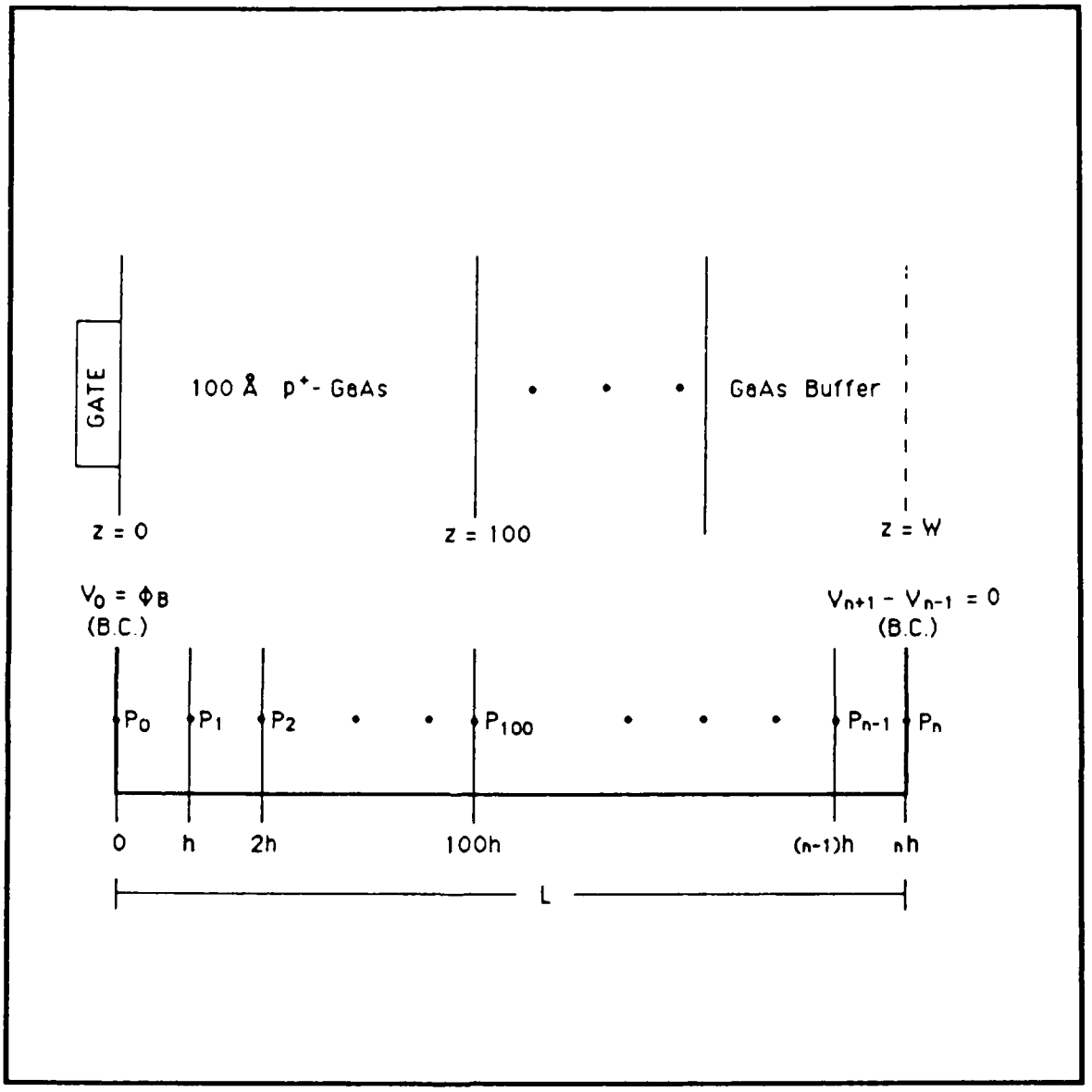


Fig. F.2 Region in the z-Plane covered by a One-Dimensional Grid of Mesh Division h. The Grid Lines Correspond to Mesh Points $P_1 = (h)$, $P_2 = (2h)$, . . . , $P_n = (nh)$, where the Region is L Units Long and $n = L/h$. The Two Boundary Conditions (B.C.) are Shown, and the Region of Interest is $0 \leq z \leq L$

where N_A is the background acceptor doping level (about $1 \times 10^{14}\,cm^{-3}$) and E_g is the bandgap of GaAs (and $E_c - E_v = E_g$). This boundary condition at W cannot be used because the value of W is not known. However, it is known that at W, $\partial V/\partial z = 0$ (called a mixed boundary value [48:856]). By using the mesh notation and (F.11b), the following is obtained:

$$V_{n+1} - V_{n-1} = 2h\left(\frac{dV_n}{dz}\right) \tag{F.16}$$

where "n" is an arbitrary mesh point. Thus from (F.16), the boundary condition at $z = L$ is $(V_{n+1} - V_{n-1}) = 0$, which can be obtained by simply adding P_{n+1} to (F.14).

A computer program was developed to plot the energy band and charge distribution diagrams of an (ESP)MODFET using the above equations (see Program 7 in Appendix C). The model uses the 65:35 rule for the conduction:valence band discontinuities as described above. The value of h was set to 1 Å (1×10^{-8} cm). Starting with $V_o = \phi_B$, an estimate was made for the value of V_1. From this and (F.14), the values of V_2, V_3, . . ., were then determined successively until an epitaxial layer (hetero) interface was reached. At this point, two boundary conditions exist. The boundary conditions are the conduction band discontinuity ΔE_c (if any) and the continuity of electrical displacement (e.g., $\varepsilon_1 E_1 = \varepsilon_2 E_2$ or $\varepsilon_1(\partial V_1/\partial z) = \varepsilon_2(\partial V_2/\partial z)$. Thus, it was necessary to add the ΔE_c (if any) at the interface and then use (F.11b) and (F.13b) before continuing the solutions of (F.14) in the next epitaxial layer, and so on. This series of successive calculations was taken up to $z = 5001$ Å past the quantum potential well (an arbitrary point where it is known that the rate of change of electric field with distance is very small) and then (F.11b) was used to see if $V_{5001} - V_{4999} \leq 1 \times 10^{-4}$ (≈ 0). The value 1×10^{-4} was taken as a convergence error minimum. It was found that since the conduction band rises very slowly past the quantum potential well, that the value of the electric field at 250 Å past the well is approximately equal to the value of

the electric field at 5000 Å past the well (e.g. $V_{251+n} - V_{249+n} \approx V_{5001+n} - V_{4999+n}$ within 0.1 percent when the guess for V_1 is correct and where n here is the distance to the end of the potential well or equivalently the beginning of the GaAs buffer epitaxial layer). After checking for convergence, a new value is selected for V_1 and the entire process repeated. The iteration continues until the convergence error minimum is reached. The results are then plotted.

As an example, Model 3 was used to plot the energy band and charge distribution diagrams of the MPD-H503 HEMT shown in Fig. 2.1. The Schottky-barrier height was taken as 0.8 eV, and the n-AlGaAs barrier layer was assumed to have been etched (recessed) to a thickness of 350 Å. The result is shown in Figs F.3 and F.4.

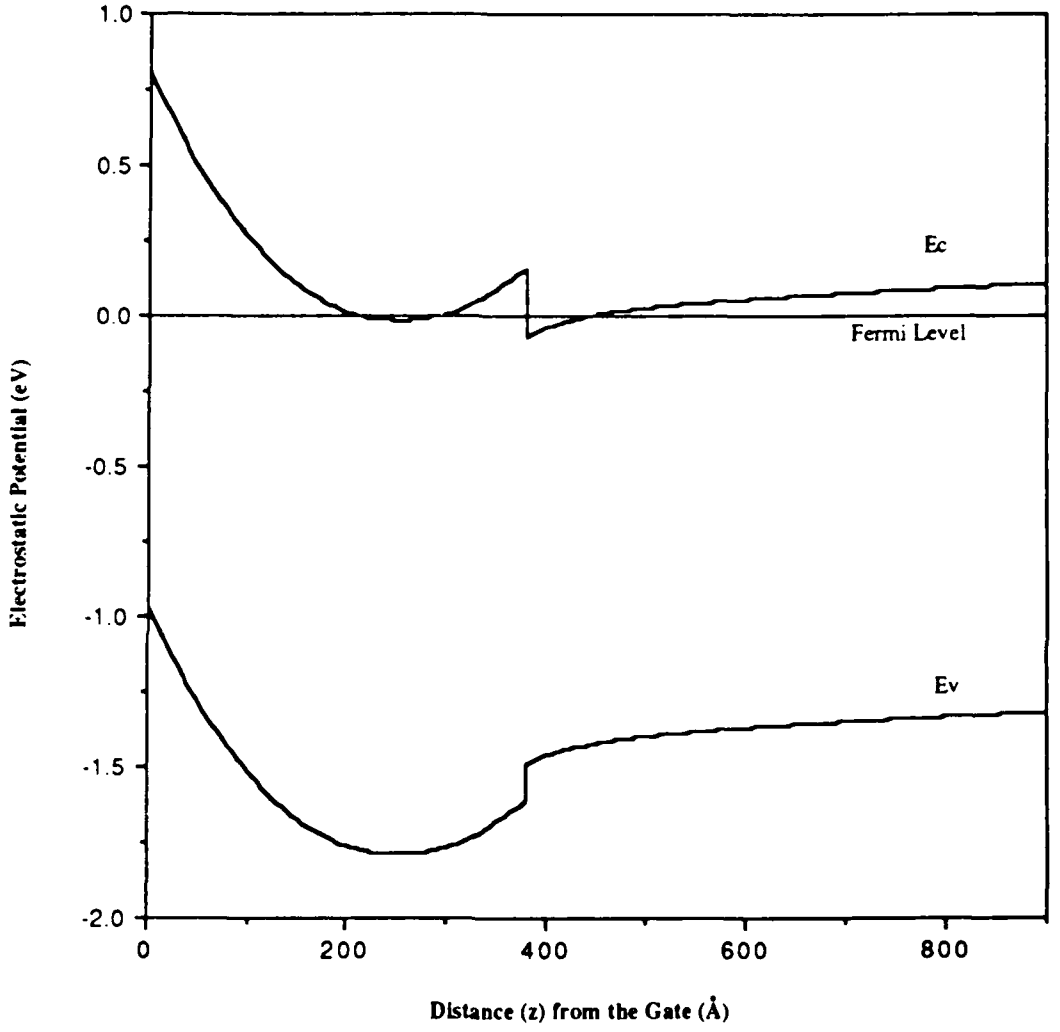


Fig. F.3 Expected Energy Band Diagram for the MPD-H503 HEMT . The Plot Values were Calculated from Model 3

MPD-H503

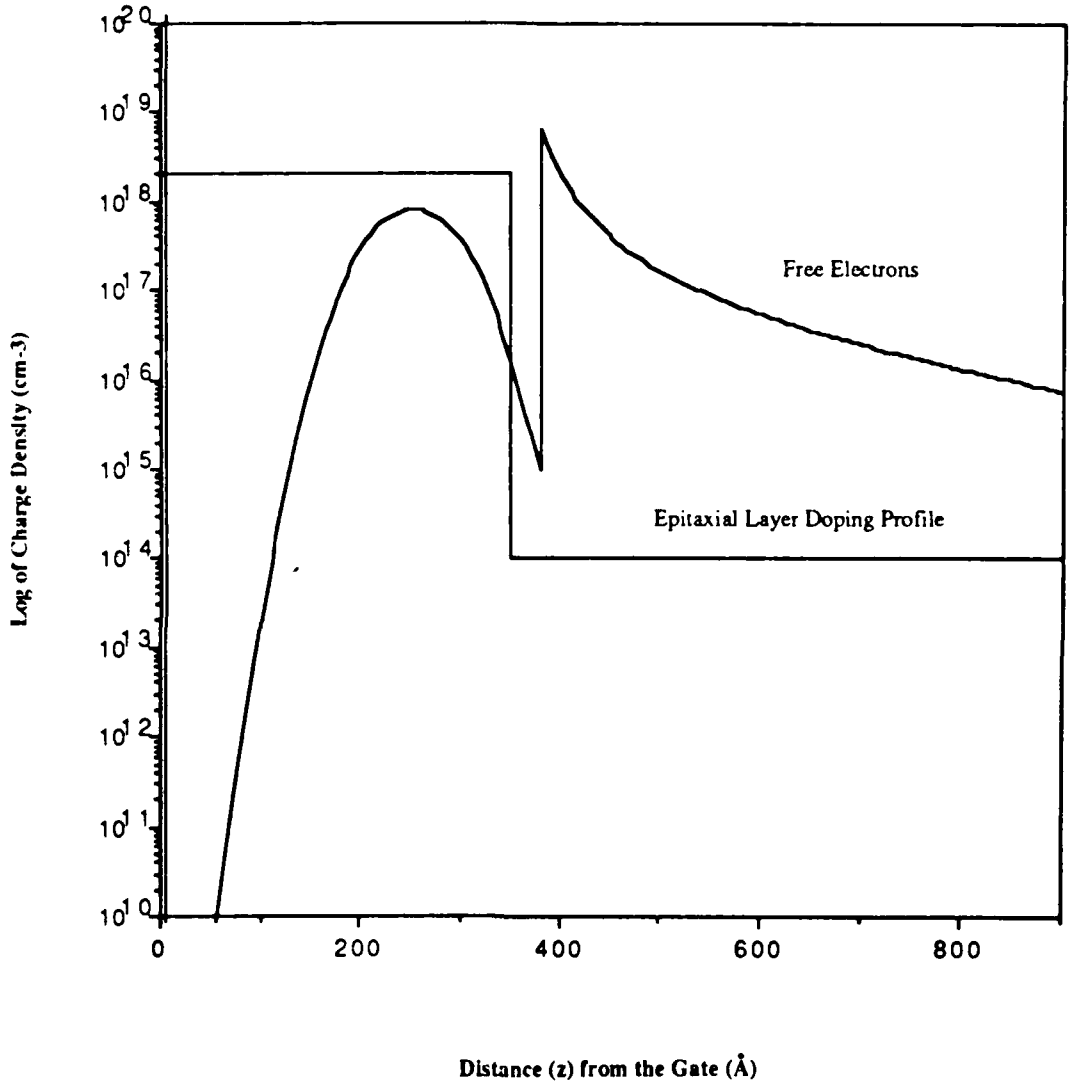


Fig. F.4 Expected Charge Distribution Diagram for the MPD-H503 HEMT . The Plot Values were Calculated from Model 3

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Enhanced Schottky-barrier $In_{0.15}Ga_{0.85}As/Al_xGa_{1-x}As$ pseudomorphic modulation-doped field-effect transistors (MODFETs) were fabricated with 1.2 μm gate-lengths on MBE-grown substrates. The effective gate Schottky-barrier height was enhanced by adding a thin p^+-GaAs layer beneath the gate. A portion of the n-$Al_{0.15}Ga_{0.85}As$ barrier layer beneath the p^+-GaAs surface layer was linearly graded from a mole fraction of 0.15 to 0.30 to further increase the effective Schottky-barrier height. MODFETs of identical dimension and doping density were fabricated without the p^+-GaAs and/or graded n-$Al_xGa_{1-x}As$ layers for comparison. The goal was to improve the MODFET's high-frequency performance by reducing the gate leakage current. The effective Schottky-barrier height was shown to increase from 0.9 to 1.6 eV for the p^+-graded samples. The extrinsic transconductance was as high as 190 mS/mm for the p^+-graded samples and 311 mS/mm for the graded control samples. The p^+-graded samples exhibited an f_T and f_{max} of 26 and 54 GHz, respectively, compared to 19 and 28 GHz, respectively, for the graded control samples. The noise figure for the p^+-graded samples was 1.7 dB at 12 GHz, compared to 1.9 dB for the graded control samples. Overall, the MODFETs with enhanced Schottky-barriers significantly outperformed control devices with unenhanced barriers. Also, this is the first time that enhanced Schottky-barriers have been successfully reported for pseudomorphic MODFETs. A first-order charge-control model was derived to design the MODFET structures by solving the Poisson equation with appropriate boundary conditions. This model is compared to the classical charge-control model based on a numerical solution of Poisson's equation and the Maxwell-Boltzmann approximation to the Fermi-Dirac distribution function. This model produces energy band and charge distribution diagrams for a given MODFET structure. The models are shown to have excellent quantitative agreement with the measured results.

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